

Reliability Evaluation of Emerging Devices

Hassan Ghasemzadeh Mohammadi

LSI, I&C, EPFL

Abstract—Fast and accurate reliability estimation of integrated circuits is an open problem. Introducing the emerging nano devices such as FinFET and Stacked Silicon nanowires makes this problem even more challenging because of higher lithography fluctuation. We discuss several previous efforts for reliable circuit design and propose a methodology for accurate reliability estimation of novel transistors.

Index Terms—Nanotechnology, redundancy, circuit reliability, Bayesian network, TCAD modeling

I. INTRODUCTION

IC designers are currently encountering serious problems such as high rate of defects and variability, power density, and design complexity due to the massive downscaling of the complementary metal-oxide semiconductor (CMOS) technology into the deep nanometer regime. Keeping on this aggressive shrinking trend is expected to reach fundamental limitations in the near future. As possible candidates to replace, several emerging nano-devices such as molecular quantum devices, Schottky-Barrier and doped silicon nanowire FETs (SNWFETs), carbon nanotube FETs (CNTFETs), and various types of double-gate and Fin-Shaped Field Effect Transistors (FinFETs) have been proposed by research community.

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exam committee: Andreas Burg, Giovanni De Micheli, David
Atienza Alonso.

This research plan has been approved:

Date: _____

Doctoral candidate: _____
(name and signature)

Thesis director: _____
(name and signature)

Thesis co-director: _____
(if applicable) (name and signature)

Doct. prog. director: _____
(R. Urbanke) (signature)

These emerging nano devices could address a number of circuit design challenges namely admirable control of short channel effects and lower off-state current; however, they also introduce new problems due to more and more fabrication process variation. There is no consent which technologies eventually either integrate with or replace CMOS-based digital logic; nevertheless, future nano-devices will certainly have high rate of fabrication defect and variability. As a result, the reliability should be added as one of the optimization parameters in the future computer aided design (CAD) tools.

Fast and accurate modeling of parameter variation and fabrication defects is an important concern in current circuit design. Currently, the accurate reproducing of the large number of devices with the same characteristics such as Threshold Voltage (V_{th}) is one of the major challenges of IC industries. The amount of physical controls, during the fabrication process of nanometer transistors, cannot be precisely determined owing to technology fluctuations. Therefore, fabrication parameters such as geometrical dimensions can be very different from their nominal values. Such variations in the fabrication parameters generate substantial fluctuations in the performance of Very Large Scale Integration (VLSI) circuits. Moreover, other sources of variations such as environmental uncertainties (mostly caused by changes in circuit operating conditions, such as fluctuations in temperature and supply voltage) and temporal variations (Such as Negative Bias Temperature Instability (NBTI), which is a key reliability issue in PMOS devices) may affect circuit performances either positively or negatively. As stated in [1], a 30% variation in effective channel length could cause over 20x fluctuations in leakage current. The variation caused fluctuation in performance may lead to a faulty state of a system or a low manufacturing yield. Thus, a new methodology of the circuit design is needed to address the non-uniform behavior of the emerging transistors across a circuit and make the final circuit more robust to the process variation and fabrication defects.

Fault and defect models play a prominent role in reliability analysis of integrated circuits. Inductive defect analysis is the procedure for developing fault models of lithography defects and fabrication fluctuations that can be applied into the higher levels of abstraction for reliable circuit design. Fault modeling for ordinary single-gate CMOS is extensively researched, and comprehensive fault models have been established. For example, bridging [2], stuck-at [3], delay [4] and stuck-open [5] faults are among these most widely used fault models for CMOS. More than 80% of the lithography and physical defects can be revealed via the stuck-at fault model [6]. With aggressive shrinking to nano regime, several types of faults cannot be revealed by employing current CMOS fault models

[7] or may completely alter their behavior in nano-devices with different technologies. The stuck-open fault (SOF) can be referred as an example of these challenging faults [8]. Shrinking geometries leads to a highly rate of the former fault models, whereas process variations increase the significance of the stuck-open, bridge and delay faults [9]. Moreover, the effects of the input variation become more significant due to the noise. While bridging, stuck-at, stuck-open and delay faults cover most of the defects in CMOS gates, it is not obvious if they comprehensively map defects in SNWT, CNTFET, and FinFET and other promising devices as well. This makes the process of fault detection more crucial and motivates designers to improve more precise methodologies for reliability analysis. The important questions that are necessary to be investigated are:

- How do the logic gates of these newly fabricated devices behave in the presence of defects and lithography fluctuations like open connections, short connections, oxide flaws, and dopants variation?
- How can we model the effects of fabrication defects and process variation for upcoming technologies in a reasonable cost?

Given these limitations, IC designers should precisely integrate reliability to the current circuit design methodologies and assess the advantages of applying fault detection and correction mechanism against their costs. Based on the rate of defects, adequate protection schemes must be utilized to achieve expected level of reliability with desired cost and/or performance. Hence, a proper balance is needed between cost and reliability especially during the early stages of design. Granularity of the fault tolerance also plays a significant role in the design of the future chips. Various scheme of fault tolerance techniques, have traditionally utilized to deal with high defect rate, must be carefully applied in different level of hierarchies to improve yields with small overhead increases [10]. Therefore, the design process of the future chips require reliable hybrid architectures, necessitating investigation of speculation and adaptivity to guarantee correct computation at low hardware and time costs.

This proposal aims at introducing a generic methodology for process variation modeling and inductive defect analysis of nano scaled devices based on TCAD simulation. Previous works utilize monte carlo (MC) simulation on the SPICE model of CMOS transistors for the purpose of reliability estimation; however, time complexity and difficulties in precise SPICE model extraction of upcoming miscellaneous transistors make this approach less interesting. Moreover, they focus on analysis a special defect of variation of specific parameter on the overall circuit design. The proposed methodology exploits TCAD simulation to realistically model the behavior of a newly designed device with respect to the potential physical variations. Then we discuss how we can effectively select the main sources of defect and variation for reliability analysis and then applying a low cost technique to estimate fault and defect tolerance of ICs.

II. SURVEY OF THE SELECTED PAPERS

Moving toward a new CAD tool which is capable of aiming reliability as one the design requirements, we need to consider the effects of process variation, as well as lithography fluctuations of the emerging devices in order to have a metric for dependability evaluation of nano-architectural circuits through simulation. This evaluation enables us to select an appropriate fault tolerant technique in different steps of circuit design. In this section, I overview three papers on reliability evaluation of digital circuit in presence of defects and variation, challenges of process variation in fabrication of emerging devices, and a novel approach reliability enhancement techniques.

A. GREDA: A Fast and More Accurate Gate Reliability EDA Tool

Based on the International Technology Roadmap for Semiconductors (ITRS) predictions, the higher probability of failure of future nano-architecture as well as higher sensitivities to noise and input variation, are going to be one of the considerable threats to the current scaling. Thus, a plentiful effort is necessary for developing electronic design automation (EDA) tool which can both estimate accurately the reliability of a circuit and integrate with other EDAs currently utilized for assessing Power consumption, timing, and hardware overhead.

The authors argue that very precise estimation of the reliability of a device is very significant due to the fact that very small error in reliability calculation is directly translated to a huge error at the system level. For instance, only 10^{-10} amount of error for gate reliability, can result in 10^{-2} for a system with 10^8 number of gates by applying a very simplistic reliability estimation approach like (1).

$$PF_{Circuit} = 1 - (1 - PF_{Gate})^{number\ of\ gates} \quad (1)$$

One of the major problem of many current EDA tool for calculating circuits problem is making use of unrealistic assumptions such as 1) $PF_{Gate} = Constant$, 2) $PF_{Gate} = 1 - (1 - PF_{Dev})^{number\ of\ dev}$, and 3) $PF_{Gate} = \sum_{i=1}^{number\ of\ dev} (-1)^{i+1} \binom{number\ of\ dev}{i} PF_{Dev}^i$.

These assumptions cause imprecise computations of circuits reliability as follows:

- Various gates are implemented using different numbers of transistors. Moreover, in gates with similar number of transistors, the topology of these devices alter the sizing of transistors thus the gates reliability.
- Overestimate failure rate of gates by applying the assumption that a single transistor failure for some input vectors will cause the entire gate to fail. Error masking property could lead to correct operation of gate when one transistor fails, or in some cases even if several transistors fail simultaneously.
- Do not provide any information about the effects of input and output voltage variation of each gate in case of a gate failure, while the variation of the voltage level can cause switching fault in consecutive gates inside a circuit. Therefore, the voltage level of the output may change according to the type of failure of devices inside a gate.

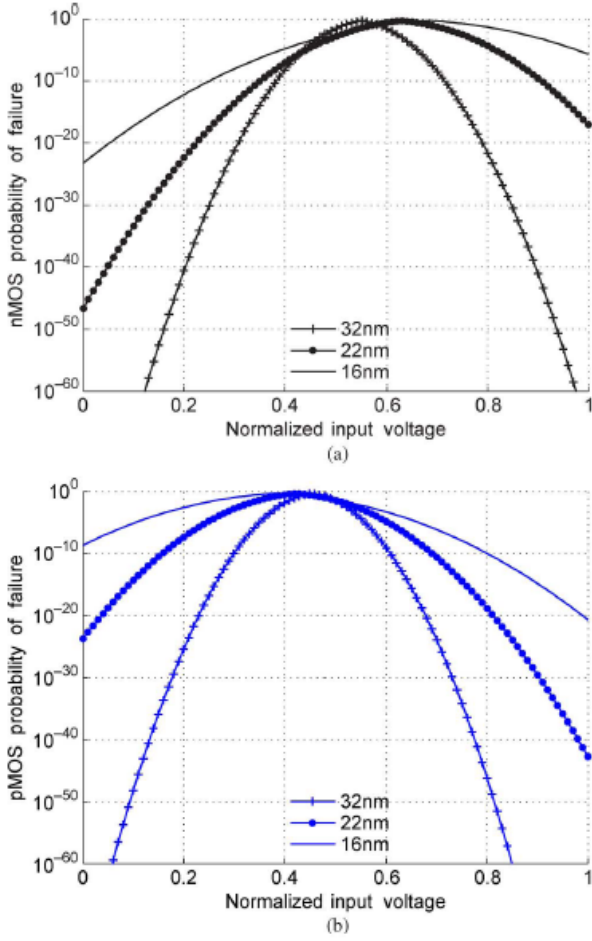


Fig. 1. Probability of failure of pMOS and nMOS transistors in the presence of gate voltage variation [11]

- To calculate the PF_{gate} , They do not consider the type of devices (i. e. pMOS or nMOS). Hence, they indicate the same PF_{dev} for different types of device which have been shown is not correct [11]. Figure 1 illustrates the probability of failures for HSPICE simulated nMOS and pMOS transistors with minimum size of 16, 22, and 32 nm.
- Finally, transistors may suffer from different types of defects and process variation such as V_{th} fluctuation as well as stuck-on and stuck-off faults. Thus, the PF_{Gate} have to be adapted appropriately with various types of defects and variation. By applying the proper value for PF_{Gate} the EDA tool enables to provide a precise estimation when multiple types of fault occur simultaneously.

To overcome the mentioned shortcomings, the authors propose a Bayesian Network (BN) based EDA tool to extract the probability of the failure for CMOS combinational circuits. Bayesian network is a probabilistic graphical model that is capable of using simplified structures in order to calculate the uncertainty of unobserved events [11]. It is directed acyclic graph (DAG) which explores the relationships among a set of random variables in order to find the joint distribution. In a graph of a Bayesian network, the nodes represent the random variable of data and the edges are referred as paths represent

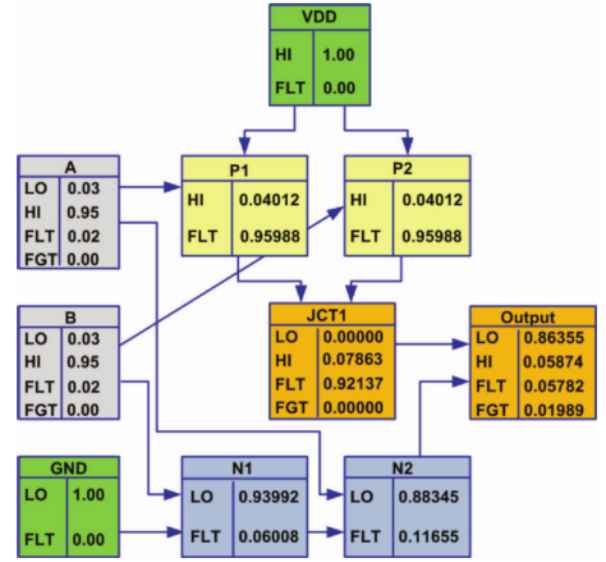


Fig. 2. BN model of a 2-input NAND gate after applying the BN inference for input "11" [12]

the conditional dependencies among the nodes. This paper, exploits different random variables such as supply voltages (VDD, GND), interconnects (Wire and wire junction node), pMOS/nMOS transistors, and finally input/output vectors. Each node contains a conditional probability table (CPT) which defines the probabilistic dependencies among distinct input combinations and the output node. Figure 2 depicts a BN model of the sample NAND-2 gate.

In order to construct the BN graph, the CPT fills by the PF quantities of each node provided by designer. Toward considering variation of the voltage for output of gates, each node in BN has the following entries: *HI* (Voltage high), *LO* (Voltage low), *FLT* (Float), and *UDT* (Undetermined). In the last two cases, the operation of the device depends upon the network of load capacitances and resistances. Additionally, to integrate the effect of process variation, variation of V_{th} as one of the important factor that can causes switching fault, has been added to the CPTs of each BN. Recent investigation has been revealed that pMOS and nMOS transistors have different switching probabilities. Therefore, four different probabilities also required to precisely model a switching fault in CPT. Finally, the authors argue that by the assumption that various possible faults and defects are *uncorrelated*, the designer can obtain appropriate CPT for each types of defects.

In order to evaluate the proposed method, BN for the different fault models (Stuck-ON, Stuck-OFF, Bridge, and Wire Break) has been created. The obtained result from calculation of reliability for six ISCA85 benchmark circuits demonstrate that the Bayesian Network based EDA tool can considerably reduce the calculation time in comparison with the well-known Monte-Carlo method.

The limitations of this work can be listed as the following:

- This EDA tool can only exploited to calculate the PF_{Gate} for traditional CMOS gates, i. e. it cannot be applied for different logic style such as pas transistor or differential

logic.

- The analytical calculation for V_{th} variation is only valid for strong inversion region, while it cannot be used for reliability calculation in subthreshold region.
- One of the major problems of the tool is that designers have to provide the quantities of probabilities for each possible defect or variation in CPTs. This means that the IC designer require another methodology in order to obtain the probability of every types of defects.
- The EDA tool only exploit the variation of V_{th} as the most prominent factor of device failures, while there is no enough discussion why they selected V_{th} among different fabrication parameters so that the variation of each can potentially change the functionality of the device.
- There is no enough explanation how this BN which used for calculating the reliability of gates are combined with other types of BN to perform reliability estimation for combinational circuit. Moreover, very small number of input vectors has been selected to perform the simulations. There is no evidence that how much the results are dependable and what the bound of error is for the selected input vectors.
- The proposed tool cannot be applied for reliability estimation of the emerging device such as FinFETs and SNWFETs because the variation analysis is based on the ordinary CMOS equations.

B. Investigation on Variability in Metal-Gate Si Nanowire MOSFETs: Analysis of Variation Sources and Experimental Characterization

Continues shrinking of the feature size raises the fluctuations of lithography process which is the main source of the variation in the newly fabricated devices. Therefore, the study of source of variation play an important role in the design of next generation integrated circuits which exploiting emerging devices. Gate-all-around (GAA) silicon nanowire FET (SNWFET) is one of the potential candidates of replacing feature CMOS generation owing to excellent control over the channel, quasi-ballistic characteristics as well as enhanced dopants transport characteristics. Due to the aggressive scaling of NW dimensions and unique structure of the device, the source and impact of the lithography variation may be completely different from the conventional CMOS devices.

The authors have divided the source of variation into two groups. In the first group they investigate the conventional source of variations which are similar to that of the planar devices. Metal-gate work function variation, gate length variation, and variation of carrier transport properties are as examples of this group. In the second group they study the new variability issues of the SNWFETs. First one is the nanowire cross-sectional variation. To evaluate this type of variation, they consider three different final cross-sectional shapes for the nanowires: Rounded with larger radius, elliptic and rectangular. Second one is lateral shape variation which is related to the nanowire line edge roughness (LER). For this case two scenarios are considered:

- type-A LER: nanowire channel has aligned center while the diameter of the nanowire varying along the channel

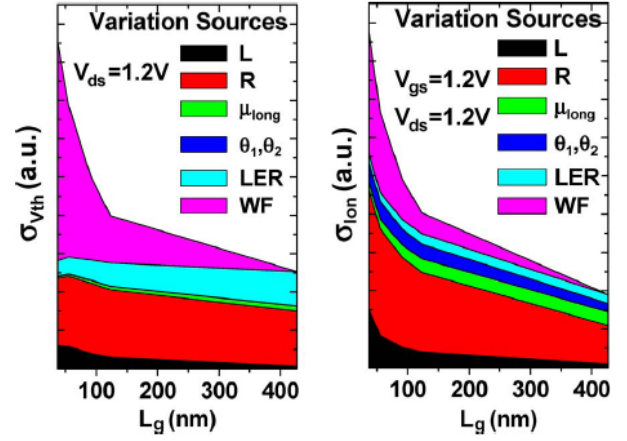


Fig. 3. Contribution of the main variation sources to V_{th} and ON-current in the SNWFET as a function of channel length (θ_1 and θ_2 are scattering mobility attenuation factors) [13]

- type-B LER: nanowire channel has a fixed diameter but varying center

Third one is random dopant fluctuation in nanowire source and drain parts. This type of variation arises from the annealing process of forming source and drain. In this case, the impurities can penetrate into to the nanowire channel and consequently decrease the length of the channel.

In order to simulate the effects of the mentioned variations, authors developed a SPICE model for GAA-SNWFET which is calibrated with the measured statistical I-V data. The variation of parameters in nanowire model is adjusted through a HSPICE monte-carlo simulation. Figure 3 depicts the contribution of the main variation sources to V_{th} and On-current in SNWFET.

The main limitations of this work are:

- The model for nanowire cross-sectional variation does not follow the real fabrication process of a nanowire formation. Therefore the mentioned shapes do not really model the effects of cross-sectional variation on nanowire.
- The variability characterization method, in this paper, relies on the SPICE model of the device. For most of the emerging nano devices with complex geometries (i.e. Ambipolar Schottky-Barrier transistors) extracting a precise spice model could be very difficult and time consuming. TCAD modeling which uses statistical data for calibration can be considered as an alternative approach.

C. Gate-Level Redundancy: A new Design-for-Reliability Paradigm for Nanotechnologies

The common technique for developing fault tolerant architectures in the face of transient or permanent faults is to exploit redundancy. Redundancy can be utilized in the form of static or dynamic. Almost all of redundancy techniques utilize voting mechanism in order to detect or mask faults of the outputs of the redundant modules. The major problem of the voter is exponential grows of its number of gates with the number of redundant modules. In order to achieve desired level of reliability in deeply nano-scaled circuits, where protection

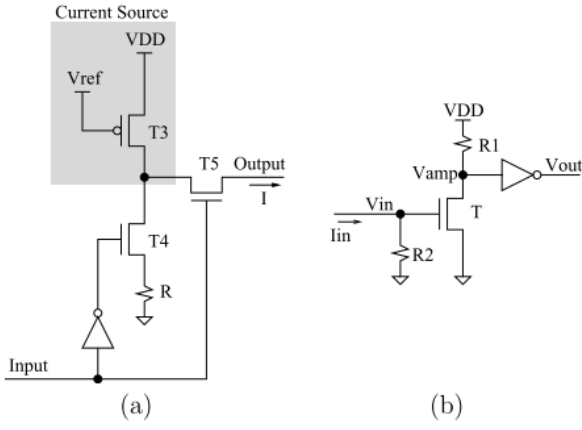


Fig. 4. Distributed voting components (a) current-based driver (b) Buffer [14]

against high rate of defects is required, a large redundancy factor is inevitable. As a result, designers need employing huge voters which impose a noticeable delay and power consumption although have reliability problem.

This paper introduces a distributed architecture for voting mechanism utilizing current based drivers, in order to convert the output voltage of each module into current signals. The authors also propose a NMR gate library based on the suggested voting mechanisms. The current signals can easily be combined to perform voting operation. Figure 4 depicts the structure of current-based driver and buffer in distributed voting. According to this figure, the resistor R_2 performs the conversion of current outputs into voltage signal. The voltage of resistor R_2 should follow the small-signal threshold of the amplifier for linear operation. Therefore, the maximum voltage of the amplifier can be obtained from (2) in which the A_v is the gain of amplifier.

$$V_{amp_{max}} = A_v N I R_2 \quad (2)$$

The reliability analysis of applying this mechanism shows that higher level of reliability can be achieved in comparison with conventional NMR. Figure 5 illustrates reliability analysis of the NMR technique with various redundancy factors for 74283 circuit.

One the main advantages of this novel voting mechanism is that the necessary current drivers and buffers are integrated within gate structures. Additionally, designing a circuit with different redundancy factor for each part of the circuit is completely straightforward which means that distributed voting is scalable for any circuit size and redundancy factor. Distributed voting is not limited to the current CMOS technology. It can be applied for different technologies and logic styles such as SNWFETs, and CNTFETs.

The limitations of this new voting mechanism can be summarized as the following:

- One of the main drawbacks of this mechanism is high sensitivity to the current drivers. In the case of failure in one current driver, the voter can produce a completely wrong result. This case happens when a transient or permanent fault causes one of the current drivers produces

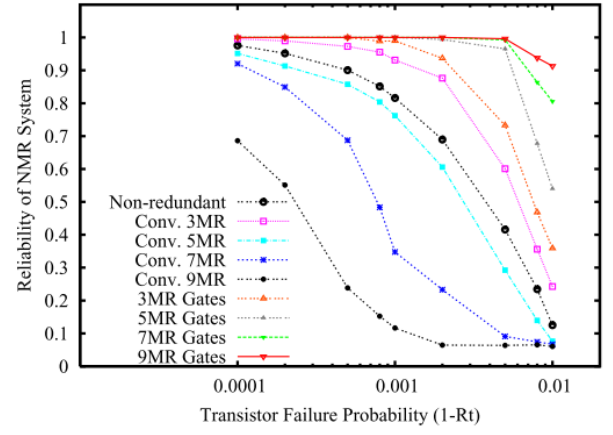


Fig. 5. Simulation results (reliability) of the NMR 74283 circuit [14]

a large amount of current. Hence, the current passes through R_2 resistor produces a voltage higher than the amplifier threshold and a wrong majority voting result is obtained. Although the authors argue that increasing the redundancy factor can diminish this erroneous event, a large redundancy factor is impossible in practice due to the very small noise margin of the voting mechanism.

- The effects of process variation on different components of the proposed buffer and drive circuit (i. e. R_2 resistor) may seriously degrade the performance of this mechanism. There is no evidence that this mechanism enables to perform adequately in face of high rate of process variation in nano scaled architectures.
- The fault model that has been used for reliability analysis is only single bridge fault between source and drain of transistors. More investigations are necessary to evaluate the reliability enhancement of this mechanism in the presence of other types of faults.
- The noise margin of the redundant circuit decreases for larger redundancy factors. Thus the application of distributed voting against conventional voltage-based voting is limited to lower amount of redundancy factor.

III. RESEARCH PROPOSAL

In this section, I will demonstrate my initial ideas about how I plan to contribute to reliability assessment of emerging devices and reliable architecture design. One goal of my research is to develop a low cost and accurate methodology for reliability evaluation of nano silicon emerging devices. Fault simulation is an important step in the iterative process of optimizing the circuit design in which exploiting a precise defect model plays a critical role. Moreover, considering all kinds of geometrical defects in the circuit simulation process impose a large computation penalty. Addition of various types of fabrication variations makes the problem more complicated. Consequently, a fast and accurate design methodology which address all of these issues is absolutely required.

The following topics and questions will be covered in my future work:

A. Extracting possible defects and variation sources according to fabrication process

One key to achieve a fast and low cost design methodology is considering the steps of fabrication process which leads us into an efficient and realistic defect/variability model. Without loss of generality, I will consider the double gate Schottky Barrier stacked nanowires (DG-SNW) as my platform device in order to deeply discuss my idea.

Due to the special geometry of a device, a number of defects arises during fabrication process are unique. The initial step is extracting the feasible potential defects and variations that perhaps arise in the layout of the device, for example various kinds of defects happen in DG-SNWs during the fabrication process. To extract the defect model, we utilize the geometry model of the DG-SNWs in order to find all open and short connections that are possible in different parts of the Device.

To complete our defect model, it is necessary to add variations of fabrication process to the geometrical defect model in each step. In the case of DG-SNWs, these variations can affect the final device at three major steps:

- *Nanowire patterning through e-beam lithography:* Nanowire patterning is achieved using HSQ which is very sensitive to variation in electron dose of the e-beam patterning and temperature fluctuation. Higher temperature reduces the pattern sharpness which directly translates to line edge roughness.
- *Nanowire formation by the Bosch process etching:* Variability, in the case of dry etching with the Bosch process, originates from various sources. One example is pattern sharpness. Pattern sharpness will influence mostly LER of the nanowires. Moreover, low pattern sharpness, in case of HSQ, will lead to a tapered nanowire stack, in which bottom nanowires growing thicker than top nanowires.
- *Gate oxide formation and polysilicon deposition:* Variability in this case mainly refers to the thickness of the grown oxide and the thickness of the deposited polysilicon. Gate oxide thickness will be influenced by the presence of contaminants on the silicon surface and its shape. This includes the surface roughness and nanowire radius.

Extracting the possible variation and defects of the target device provides the opportunity of finding effective defect model based on complexity and accuracy.

B. Defect model extraction for target device

Accurate and low cost simulation of the extracted possible defects and variation is very critical. As conventional electronic devices approach a limit for improvement, future device modeling and simulation must go beyond the conventional models to tackle these challenges as well. TCAD simulation provides a precise prediction of device parameters based on finite-element physical model simulation. Along with the high level of accuracy due to considering quantum effects, TCAD simulation provides the opportunity to design and simulate devices without complete fabricating of a new device. Consequently, to measure the impacts of the variation in physical parameters of the device TCAD simulation is proposed. The

challenging part of this step is calibrating the a few parts of the model such as channel with measured Statistical Data.

In order to reduce the computational complexity and design corners, selection of major defects and physical parameters that greatly contribute to the functionality of the device must be performed. Among feature selection methods, the principal component analysis (PCA) is an appropriate candidate to achieve this goal. PCA is a mathematical method that applies an orthogonal transformation to convert observations of possibly correlated variables into a set of values of linearly uncorrelated variables called principal components. The number of principal components is less than or equal to the number of original variables. The principal components are sorted with respect to the magnitude of possible variance. The components with major contribution to variance of observations are exploited to reconstruct observations with tiny loss of information. Thus the desired number of principal component can be selected according to the desired accuracy.

C. Improving a methodology for reliability computation and reliable circuit design

Trade off between time complexity and accuracy is the greatest challenge of reliability calculation models. With aggressive moving toward deep nano-scaled devices, the demand for fast and accurate reliability computation techniques is increased. Unfortunately, most of these techniques can not consider a complete defect and variation model of the target device. To the best of my knowledge, almost all of the previous techniques enable to do computation for traditional CMOS devices. On the other hand the gate level or architecture level techniques usually do not consider the variation of input signal, effects of noise and signal degradation of logic gates. Therefore the accuracy of the results is not acceptable for nano-scaled circuits despite their very low time complexity. There is a major demand for a fast highly accurate mathematical model which is capable of covering all mentioned drawbacks. Recently, Bayesian network and Markov logic network have introduced in reliability community as two powerful models for reliable CMOS circuit design; however, the current proposed technique based on these model only are capable of performing reliability analysis for very small circuits. Therefore following item should be investigated in my work:

How I can develop a model for a medium or big size circuit? Which types of sampling methods should be applied to make the time complexity of the model reasonable with guaranteed bound of error? How I can devise a model which can be used for both sequential and combinational circuits?

BN has the capability for activity estimation of a circuit. As a result, it can be strong candidate that can merge power and reliability metrics. The integration of design requirement such as reliability, delay, power consumption and area in a CAD tool for emerging transistors would be the final goal of my feature work.

IV. CONCLUSIONS

In this write-up I presented a summary of three papers that give a broad overview of challenges in the field of reliable

circuit design. Moreover, common drawbacks which are related to this work highlighted. Finally a low cost methodology presented for extracting a precise defect and variation model of future nano-devices.

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