iNoCs: Networks-on-Chip

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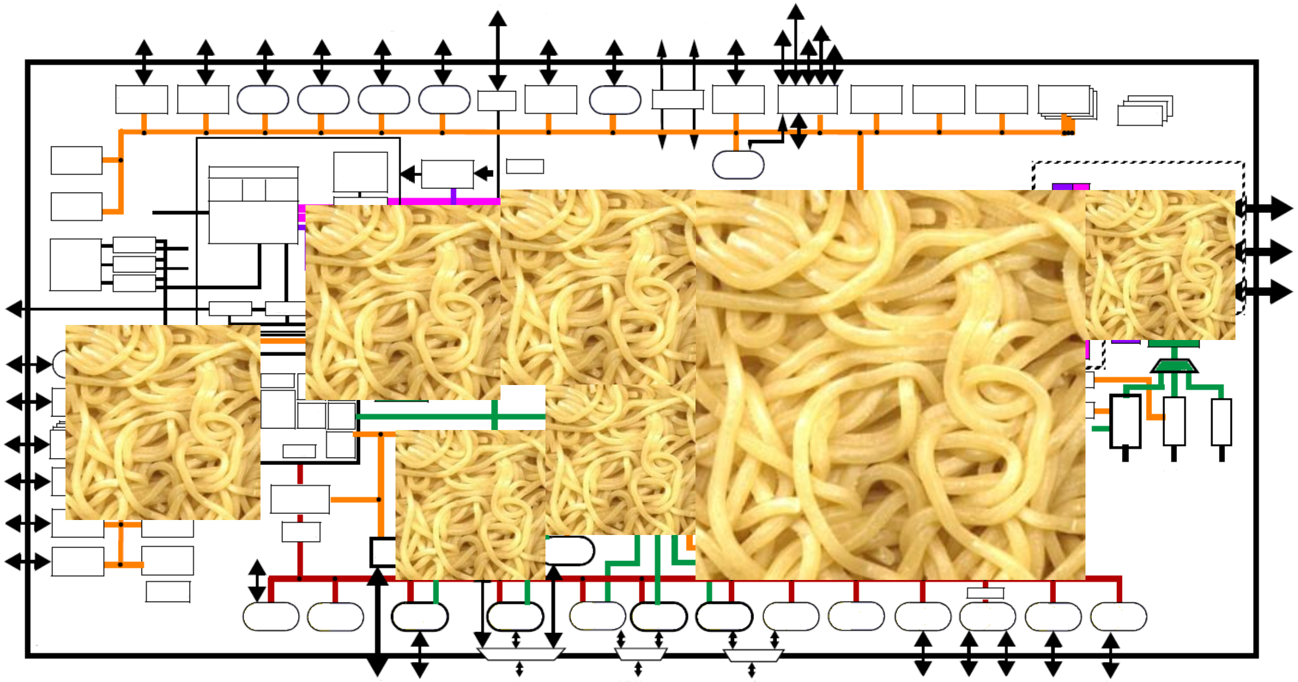
Device and Chip Evolution

- Evolution possible thanks to powerful chips
  - System-on-Chip paradigm
  - Complexity moving from whole device to chip
  - 2X on-chip processing elements every 18 months

Chip Communication Requirements

Tomorrow

The Chip Interconnection Problem



Chip for mobile multimedia apps (under NDA)

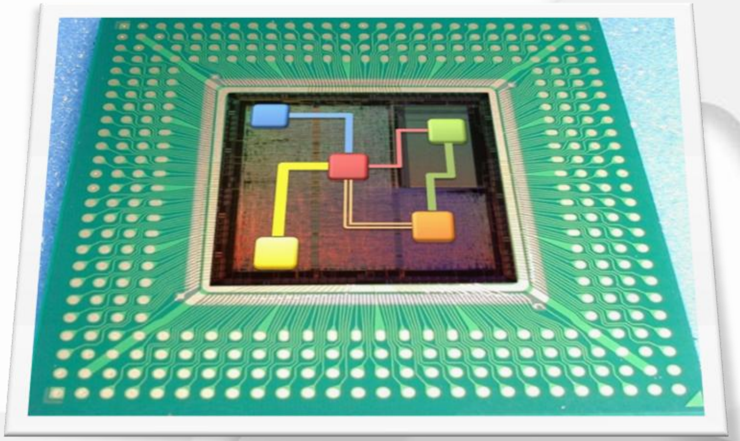
Chip Makers

- Interconnect is becoming major bottleneck
  - Unstructured wiring, large power consumption / area, poor performance
  - Long design and verification → ~ 2 years time to market (89% late!)

Source: Numetrics Management Systems

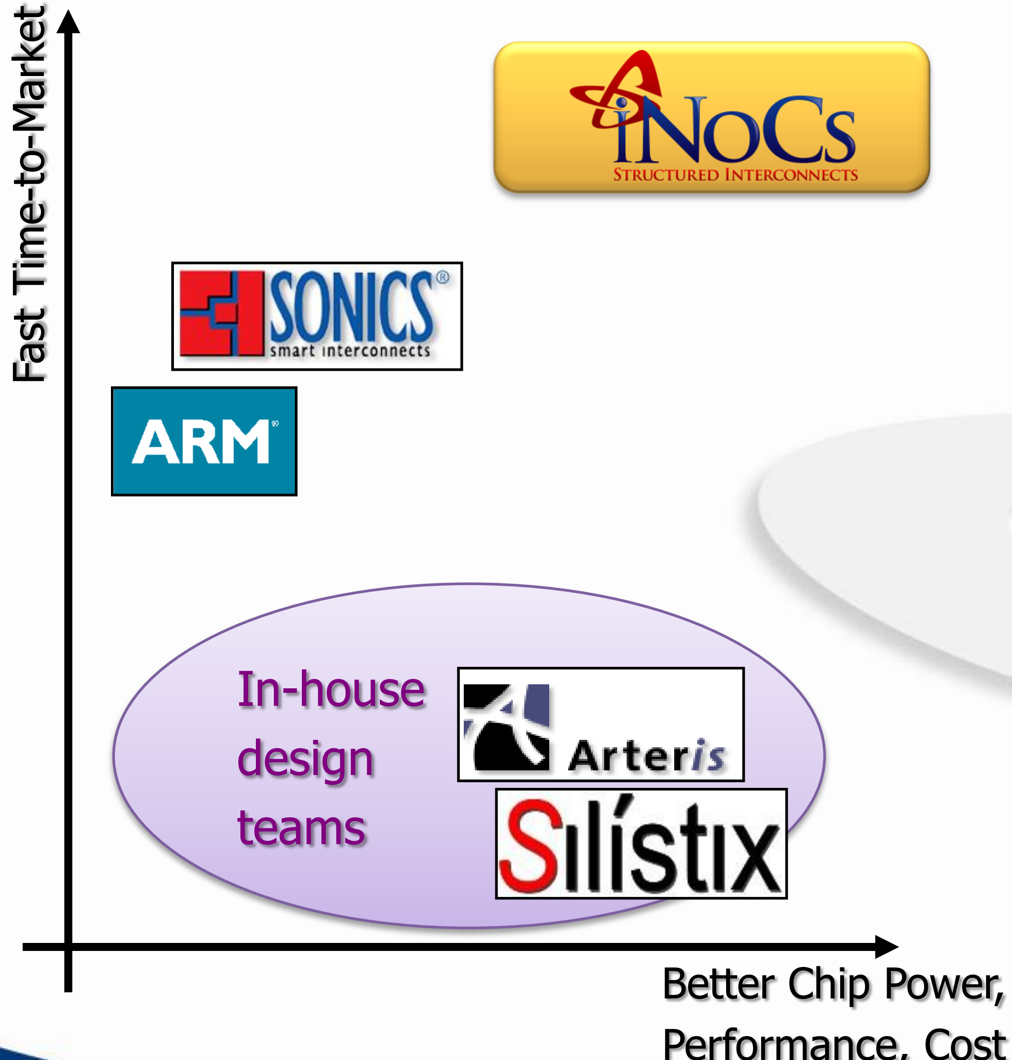
Networks-on-Chips

- Networks-on-Chips: Internet at the chip scale
- iNoCs provides
  - Hardware description (IP)
  - Design tools



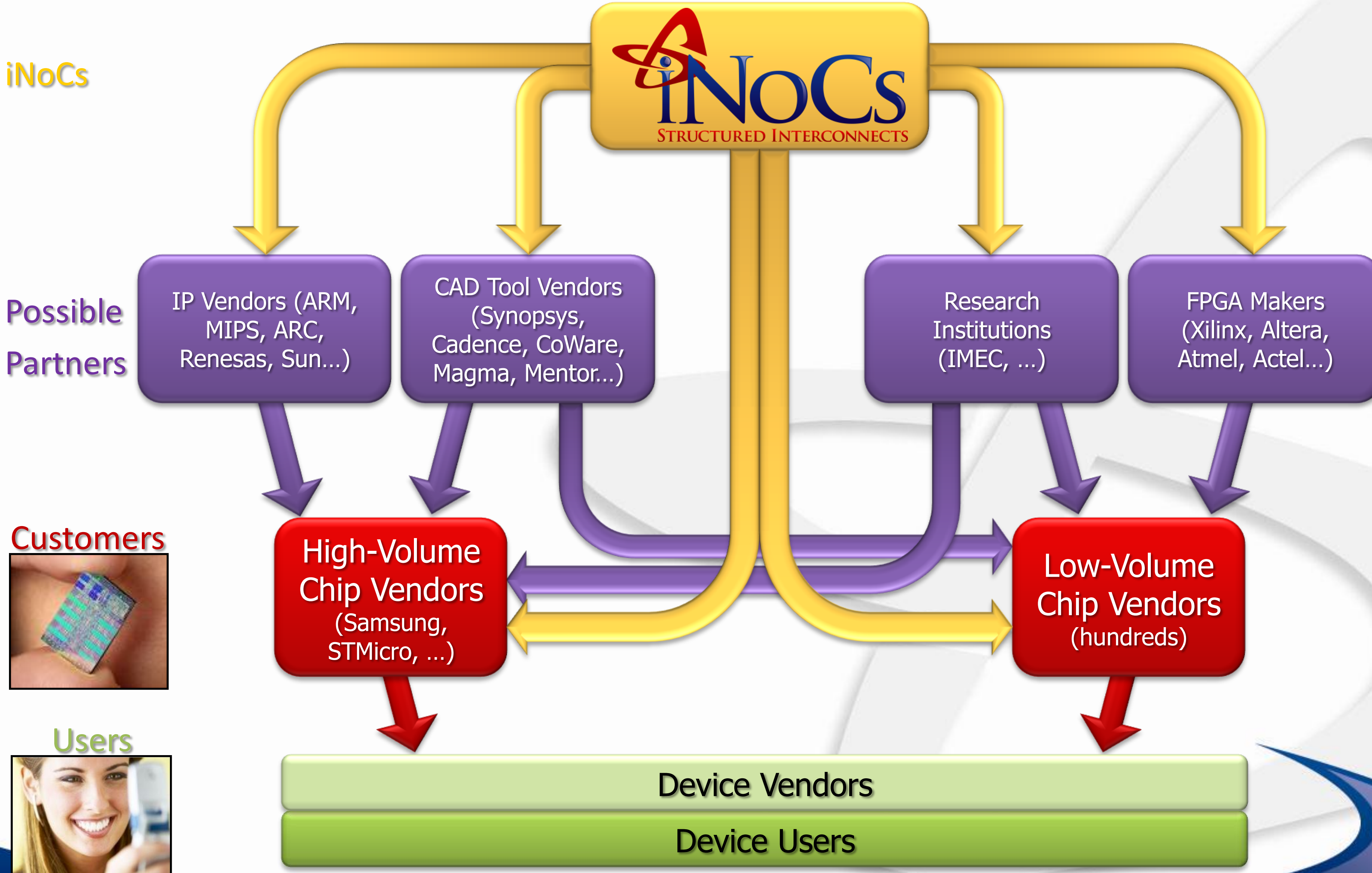
	With iNoCs	Advantage
Bandwidth	**10x better**	Faster chip
Energy Efficiency	**50% better**	Longer battery duration
Wiring Area	**4x better**	Cheaper manufacturing
Predictability	**3.5x better**	Shorter time-to-market
Design Effort	**vastly decreased**	Fewer designers needed

Competitive Landscape



- Uniquely positioned: cutting edge IP library plus front-end CAD, plug-in into existing tool flows. Best-in-class flow
- Market size today for interconnects: $150 million
  - IP vendors (Sonics: $17M)
  - In-house teams

Business Model



TEAM

Founders & Scientific

Federico Angiolini, VP Eng
- PhD, Bologna U

Srinivasan Murali, CTO
- PhD, Stanford U

Antonio Pullini
- Researcher, EPFL

Luca Benini
- Professor, Bologna

Giovanni De Micheli
- Professor, EPFL

Business Advice & Mgmt

Massimo Vanzi, CEO
- 30 years of management experience

Claudionor Coelho
- Professor, entrepreneur, VP Eng at Jasper DA

Heinrich Meyr
- Professor, Chief Scientist at CoWare

Years working together
Pioneers of NoCs
Academic awards

Plus part-time developers

Timeline

Demonstrators Prototypes Patents	NoC Infancy Design services	NoC Awareness IP license, bundle tools	NoC Maturity IP license, tool license

2007-8	2009	2010	2011	2012	2013

Clients	**Initial contacts**	**1 design** **1 customer**	**3 designs** **2 customers**	**9 designs** **4 customers**	**22 designs** **8 customers**	**40 designs** **15 customers**

Financial Outlook

	2007-8	2009	2010	2011	2012	2013
Revenue (US$ million)	0.15	0.75	2.88	12.1	31.4	
Gross Margin		-71.3%	14.4%	42.4%	50.4%	
Net Profit (US$ million)	0.08	-1.6	-2.0	-0.5	5.4	
Headcount	8	13	22	46	82	
Free Cash Flow (US$ million)	-0.08	-1.6	-2.5	-2.0	3.0	
Funds Required (US$ million)	2.0		5.0 (Q1)			

Investment Offering

- Current setup:
  - 90-95% owned by 4 founders
  - Negotiation with EPFL (5-10% equity bracket, TBD)
- Seed Funding Round A (2009):
  - Amount invested: US$2 million, pool of seed investors
  - Team expansion, customer contacts, patents, product strengthening
- VC Funding Round B (late 2010/early 2011):
  - Amount invested: US$5 million, one or more VCs
- Exit strategy: most likely is acquisition
  - IP, tool, silicon or device vendor: e.g. ARM, Synopsys, Xilinx, Apple

Thank You

iNoCs

Structured Interconnects

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