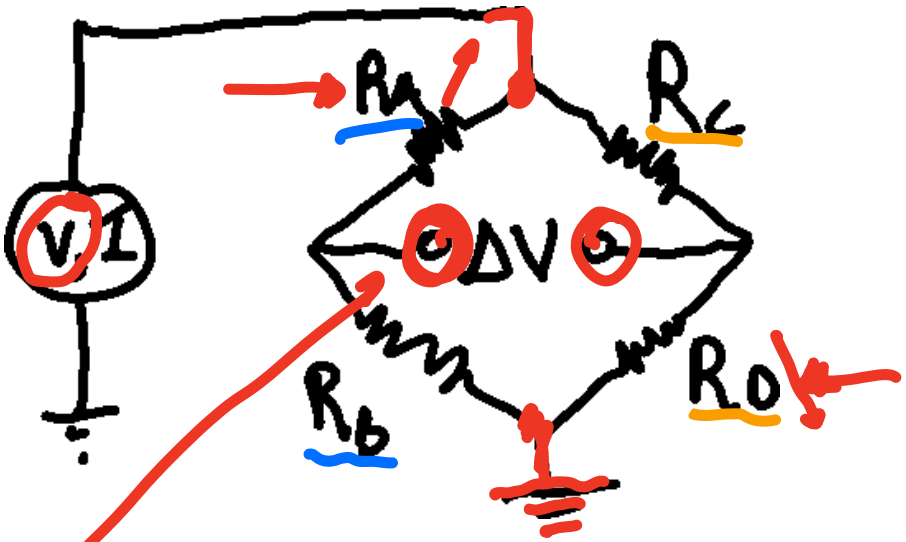
Instrumentation amplifiers, load-cell amplification, a review of the experiment, current measurement and some current sources

Week 7: AoE 7.09-7.12; 15.03

The Wheatstone bridge



Suppose we have a constant V bridge excitation. Then the total current passing through the bridge is:

$$V_0 = (R_A + R_B) \| (R_C + R_D)\, I$$

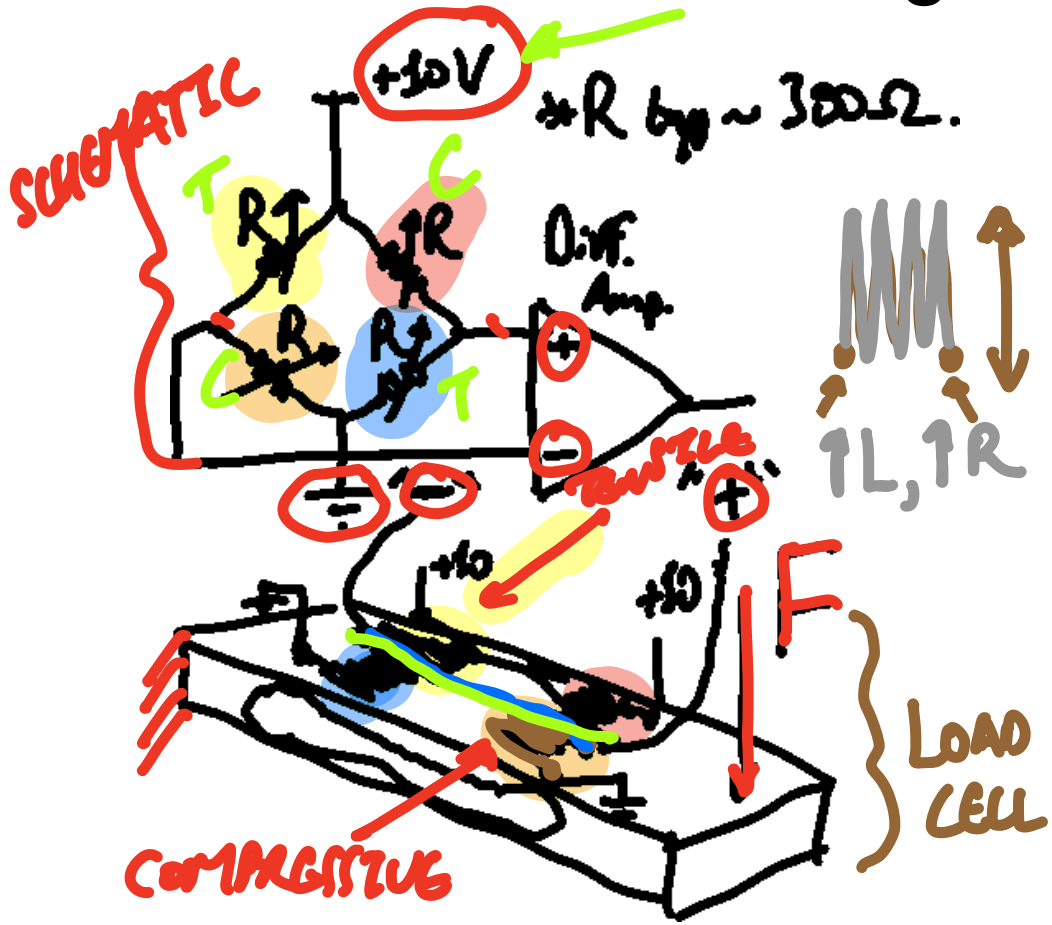
For simplicity, and to get an idea of how this bridge works, let's assume that both dividers have an equal resistance, and furthermore that all resister values are identical. Then $\Delta V = 0$.

Now, consider a case where R_A increases by an amount dR, and R_D decreases by dR.
In this case, the current passing through the two halves of the bridge (each a divider!) is no longer identical. In fact, the left current is: $V/(R_A + dR + R_B)$, while the right current is $V/(R_C + R_D - dR)$.

Thus, the voltage on the left is $R_B * V / (R_A + dR + R_B)$, and on the right, $(R_D - dR)*V/(R_C + R_D - dR)$, and after a significant amount of algebra, we find to leading order that $\Delta V \sim 2\, dR$ (the exact calculation you can do if you like!)

Fundamentally, this circuit becomes ***non-linear*** when dR becomes large compared with all the R in the bridge.

A load-cell circuit consisting of strain gages in the Wheatstone-bridge configuration:



Upon application of force, F, the strain gauges respond by changing their resistance. Under *compression,* the resistance *decreases;* under *tension,* the resistance *increases.*

Thus we can quickly see that the differential voltage will systematically change in response to applied force, as the v-dividers formed by the strain gauges in each side of the load cell will change their primary voltage values in a levered-fashion.

Nevertheless, the mean value sits around **5 V!**

→ COMMON-MODE VOLTAGE

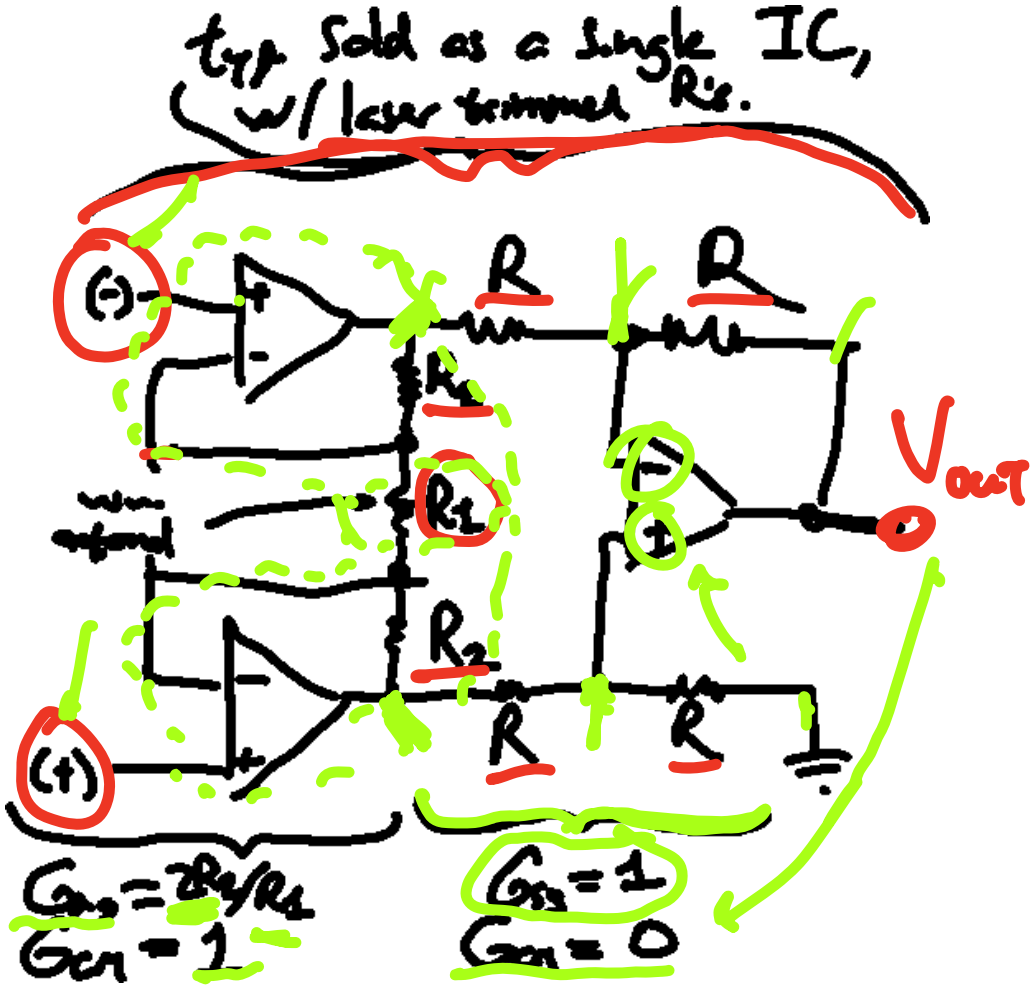
Often we are tasked with the measurement of a transducer's output

The main challenge addressed by instrumentation amplifiers is *high rejection of common-mode voltage (CMRR)*

The high CMRR is necessary because often transducers (such as load cells) have high common-mode signals (of order several V), while the signal of interest is a differential signal in the mV-scale.

If we want a 0.1% accuracy of a mV signal, say, then we must reject 5 V-common-mode down to the microvolt level (!) this corresponds to a rejection of over a million times the common-mode!

How can we achieve this?

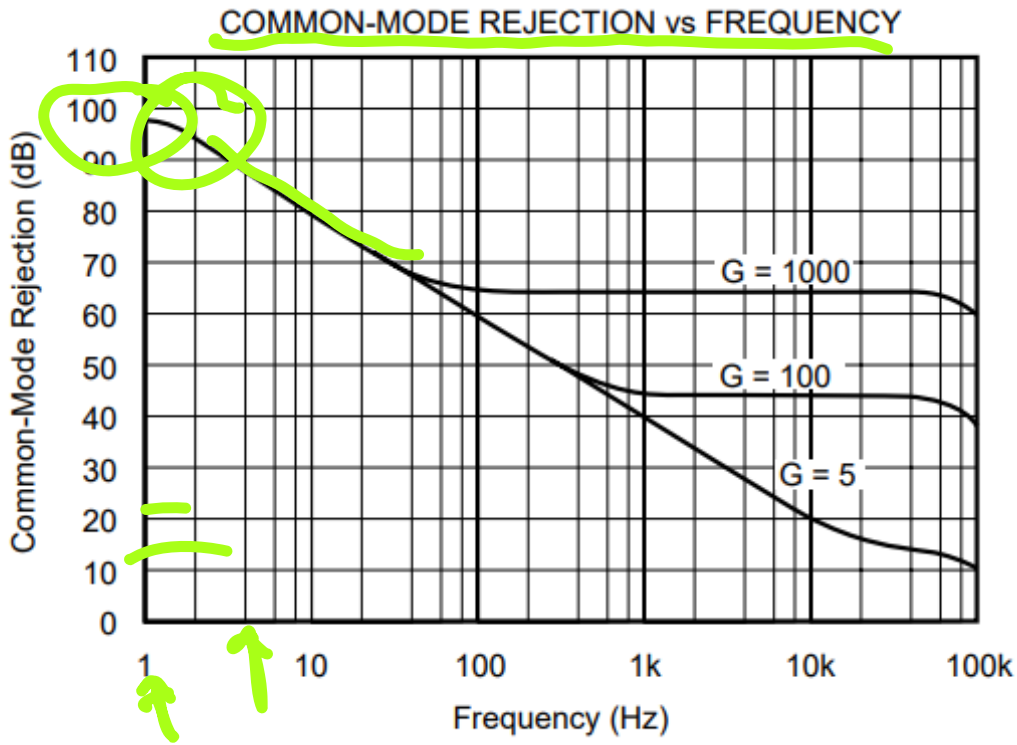


The previous circuit should look familiar from the handout on instrumentation amplifiers.

These are useful devices for discarding common-mode signals!

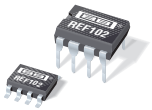
A word of caution on CMRR in INAs: see from the INA 122 datasheet:

CMRR drops at high-frequency!



Precision Voltage sources: REF 102

High CMRR: INA 122



SBVS022B – SEPTEMBER 2000 – REVISED JUNE 2009

10V Precision Voltage Reference

FEATURES

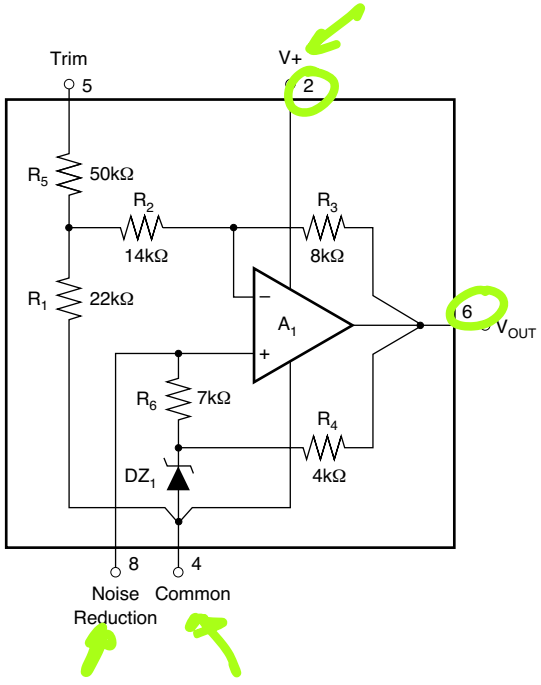
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μV_{PP} typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: PLASTIC DIP, SO-8

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETER
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max C-grade over the industrial temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single-supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.



ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage	+40V
Operating Temperature	
P, U	–25°C to +85°C
Storage Temperature Range	
P, U	–40°C to +125°C
Short-Circuit Protection to Common or V+	Continuous

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

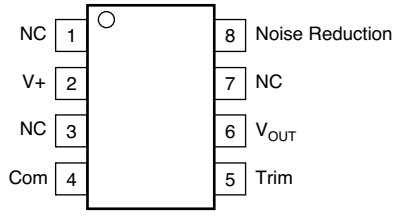
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAX INITIAL ERROR (mV)	MAX DRIFT (PPM/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
REF102AU	±10	±10	SO-8	D	REF102AU
REF102AP	±10	±10	DIP-8	P	REF102AP
REF102BU	±5	±5	SO-8	D	REF102BU
REF102BP	±5	±5	DIP-8	P	REF102BP
REF102CU	±2.5	±2.5	SO-8	D	REF102CU
REF102CP	±2.5	±2.5	DIP-8	P	REF102CP

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

Top View **DIP, SO**



NC = Not Connected

ELECTRICAL CHARACTERISTICS

At T_A = +25°C and V_S = +15V power supply, unless otherwise noted.

PARAMETER	CONDITIONS	REF102A			REF102B			REF102C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE											
Initial	T_A = 25°C	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature [1]				10			5			2.5	ppm/°C
vs Supply											
(Line Regulation)	V_S = 11.4V to 36V			2			1			1	ppm/V
vs Output Current											
(Load Regulation)	I_L = 0mA to +10mA			20			10			10	ppm/mA
	I_L = 0mA to –5mA			40			20			20	ppm/mA
vs Time	T_A = +25°C										
M Package			5			✻			✻		ppm/1000hr
P, U Packages [2]			20			✻					ppm/1000hr
Trim Range [3]		±3			✻			✻			%
Capacitive Load, max			1000			✻			✻		pF
NOISE	0.1Hz to 10Hz		5			✻			✻		μV_{PP}
OUTPUT CURRENT		+10, –5			✻			✻			mA
INPUT VOLTAGE RANGE		+11.4		+36	✻		✻	✻		✻	V
QUIESCENT CURRENT	I_{OUT} = 0			+1.4			✻			✻	mA
WARM-UP TIME [4]	To 0.1%		15			✻			✻		µs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		–25		+85	✻		✻	✻		✻	°C

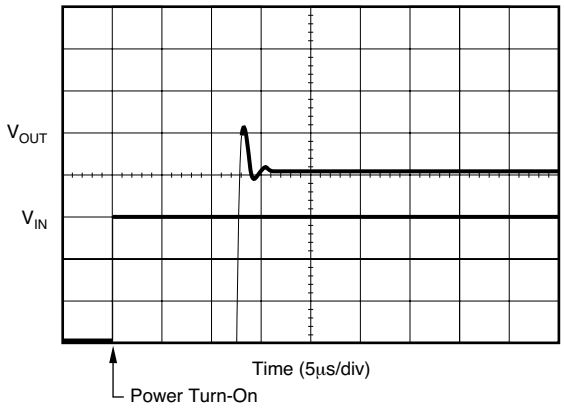
✻ Specifications same as REF102A.

NOTES: (1) The *box* method is used to specify output voltage drift vs temperature; see the Discussion of Performance section.
(2) Typically 5ppm/1000hrs after 168hr powered stabilization.
(3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details.
(4) With noise reduction pin floating. See Typical Characteristics for details.

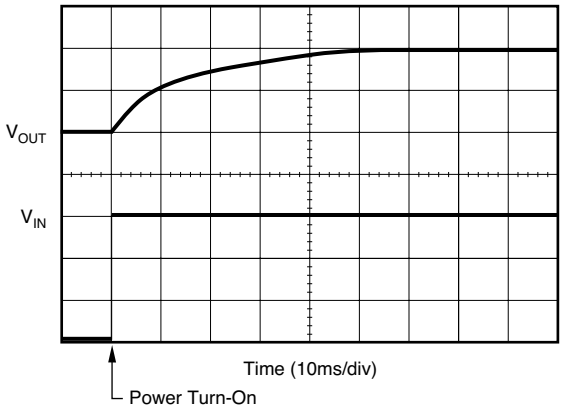
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +15V, unless otherwise noted.

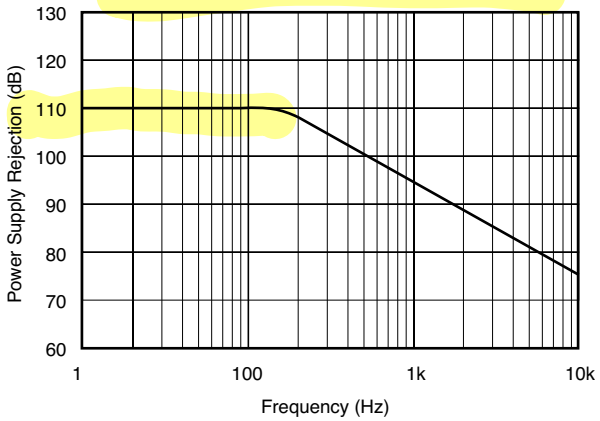
POWER TURN-ON RESPONSE



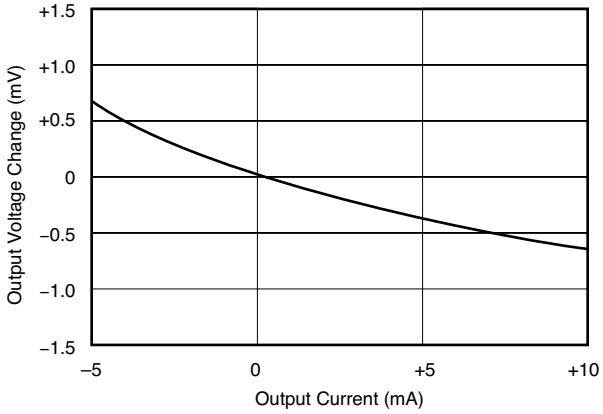
POWER TURN-ON RESPONSE with 1µF C_N



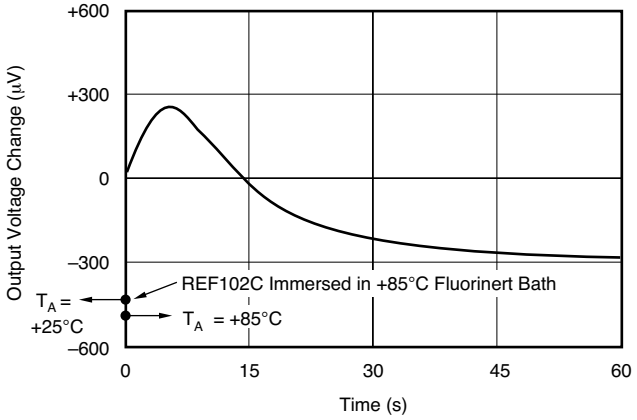
POWER SUPPLY REJECTION vs FREQUENCY



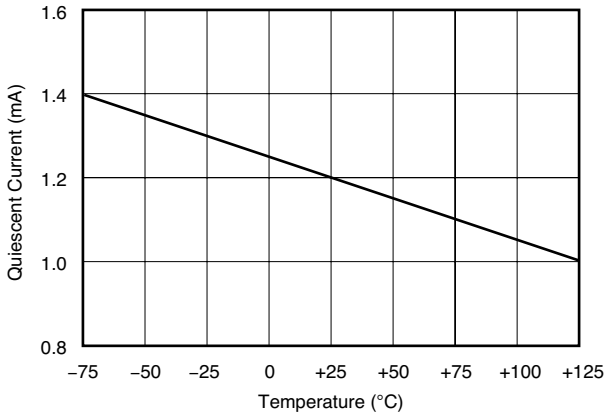
LOAD REGULATION



RESPONSE TO THERMAL SHOCK



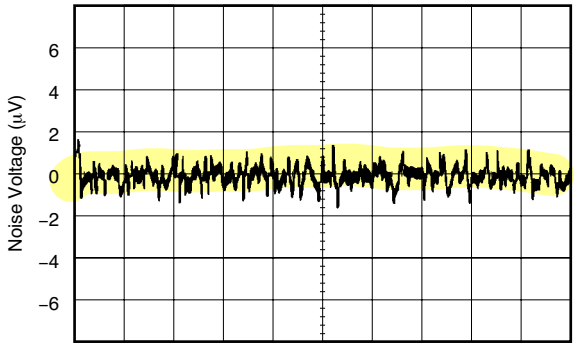
QUIESCENT CURRENT vs TEMPERATURE



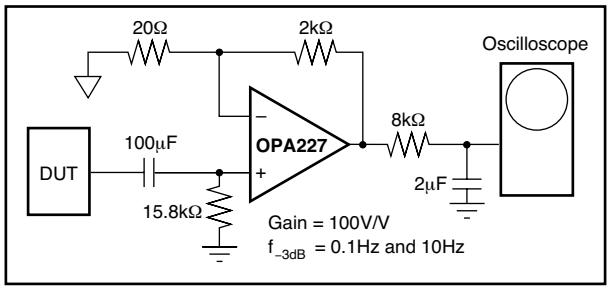
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +15V, unless otherwise noted.

TYPICAL REF102 REFERENCE NOISE



Low Frequency Noise (1s/div)
(See Noise Test Circuit)



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1, op amp A_1, and resistor network $R_1 – R_6$.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1. R_1, R_2, and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4. R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the temperature coefficient (TCR) of of R_5 closely matches the TCR of R_1, R_2 and R_3 , the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the *butterfly method* and the *box method*. The REF102 is specified by the more commonly-used *box method.* The *box* is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not known, either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CU as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The *box* height, V_1 to V_2, is 2.75mV.

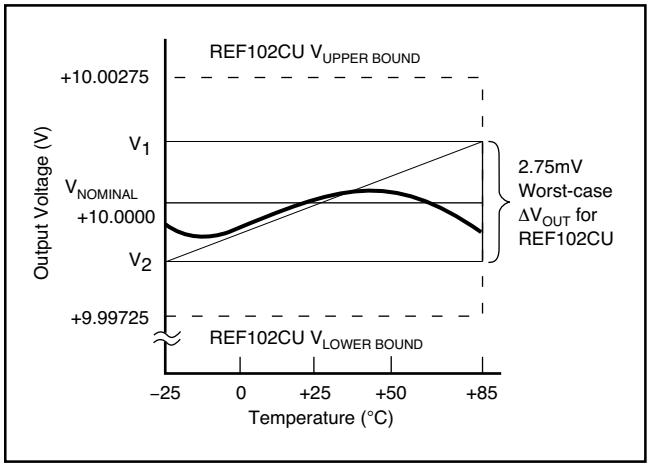
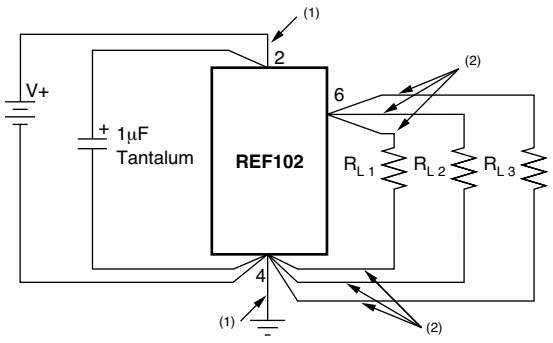


FIGURE 1. REF102CU Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated, being sure to minimize interconnection resistances.



NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

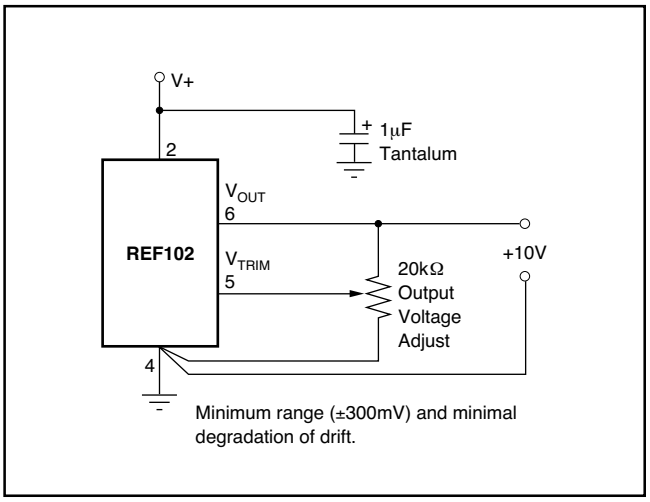


FIGURE 3. REF102 Optional Output Voltage Adjust.

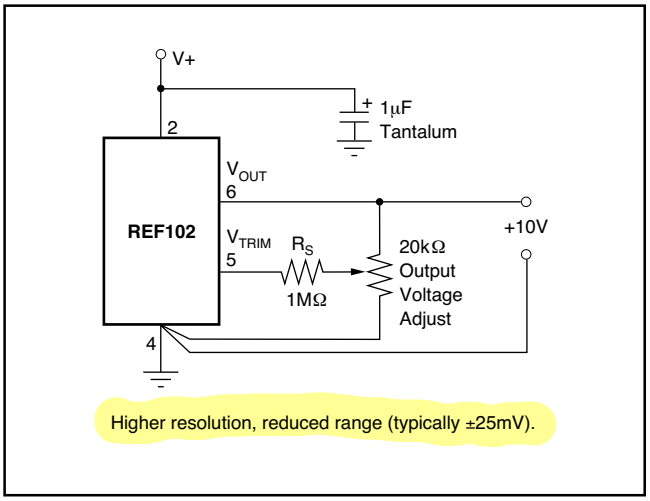


FIGURE 4. REF102 Optional Output Voltage, Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low-pass filter with R_6 (refer to the figure on page 1) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1μF noise reduction capacitor on the high-frequency noise of the REF102. R_6 is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about $800\mu V_{PP}$ to under $200\mu V_{PP}$. If further noise reduction is required, use the circuit in Figure 14.

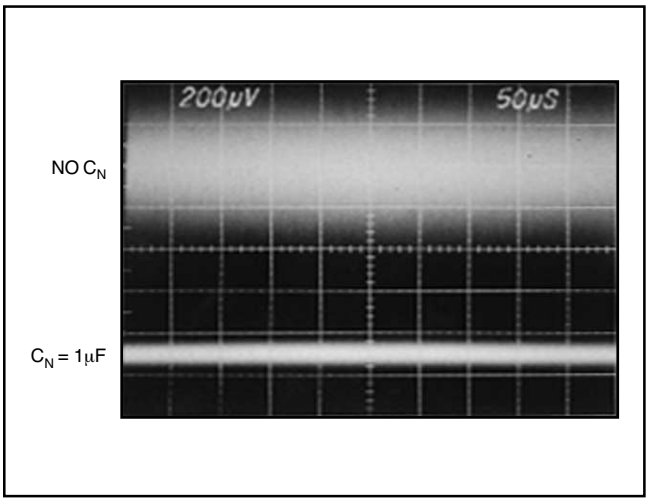


FIGURE 5. Effect of 1μF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz)

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

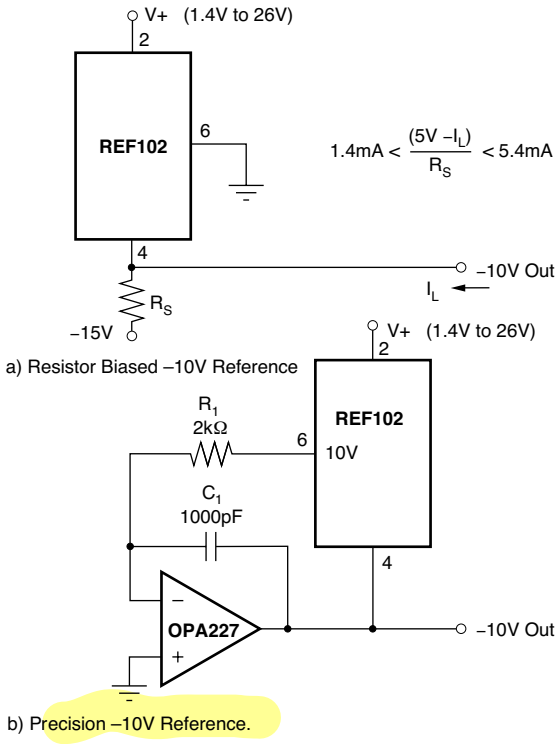


FIGURE 6. –10V Reference Using a) Resistor or b) OPA227.

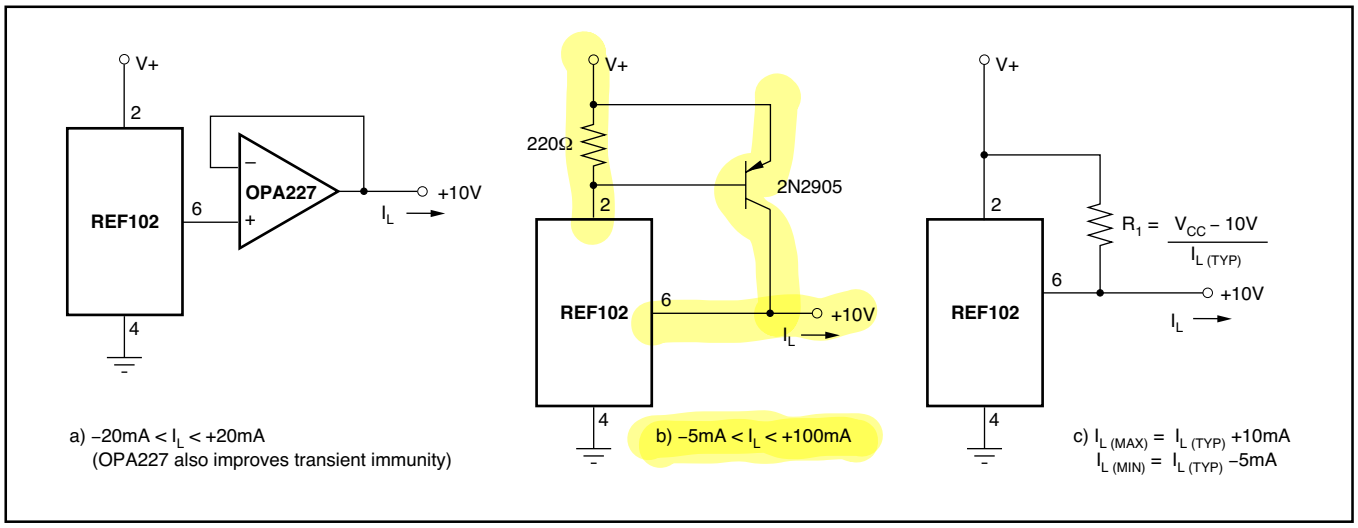


FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L\,(TYP)}$ +10mA, –5A.

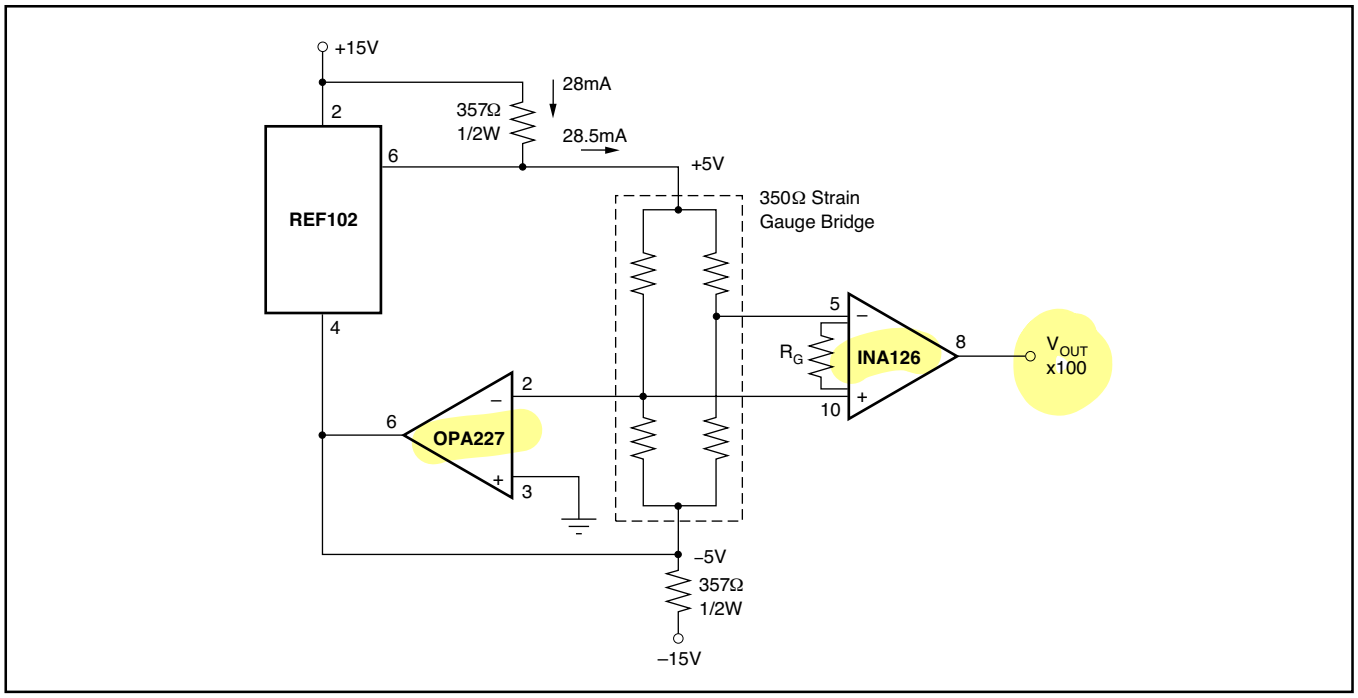


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

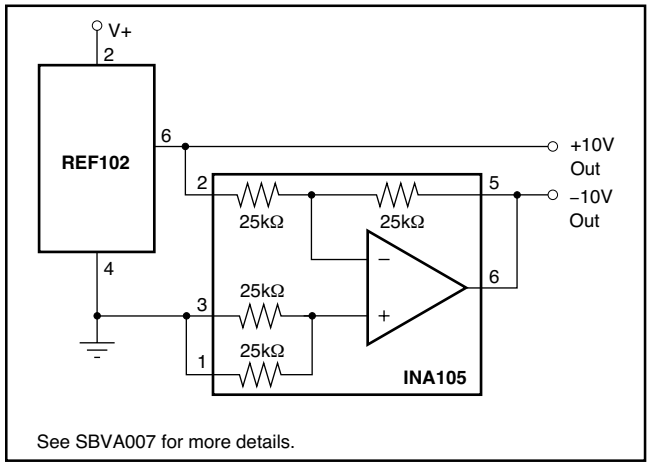


FIGURE 9. ±10V Reference.

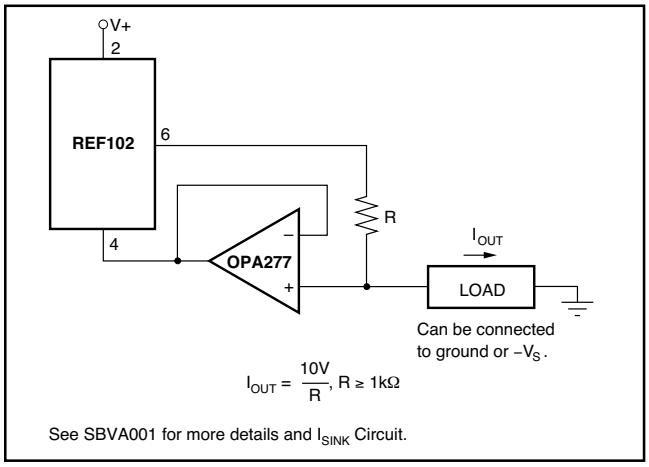
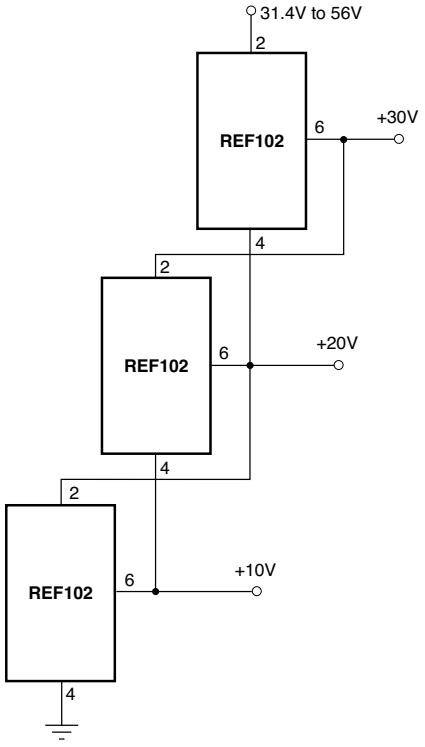


FIGURE 10. Positive Precision Current Source.



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26, where *n* is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

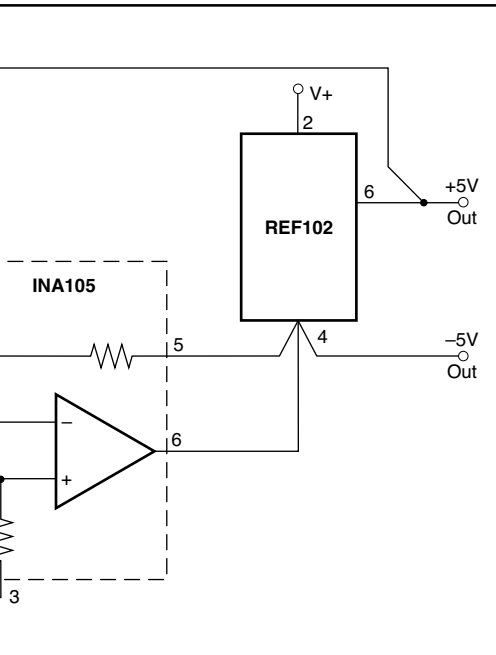


FIGURE 12. ±5V Reference.

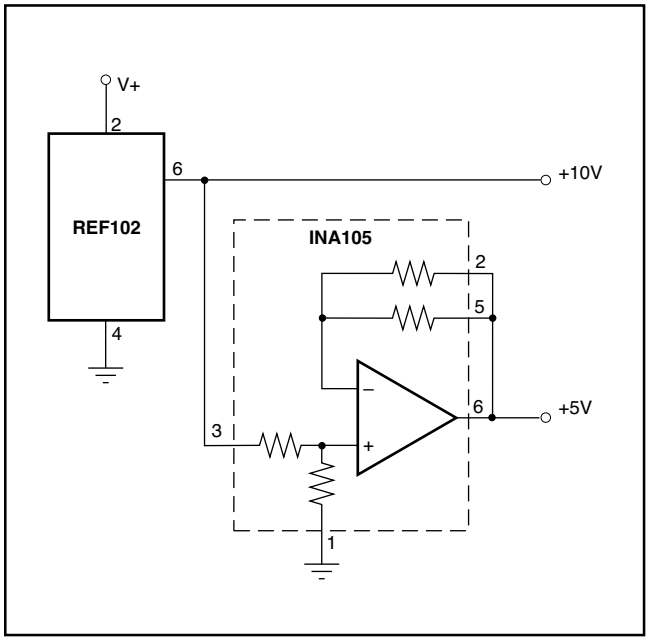


FIGURE 13. +5V and +10V Reference.

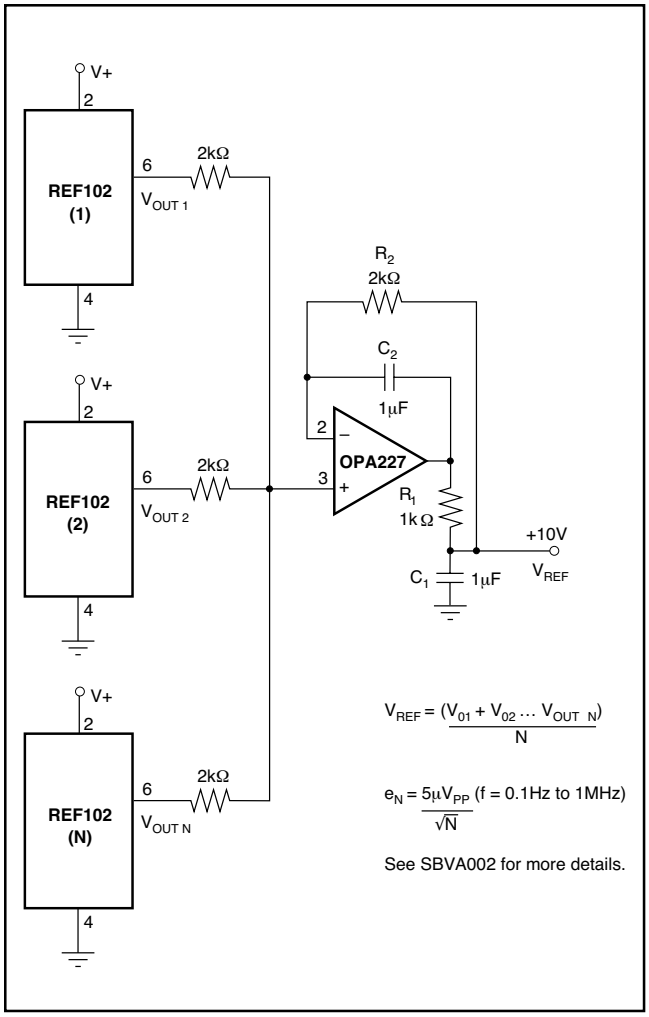


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
6/09	B	2	Absolute Maximum Ratings	Deleted lead temperature rating.
			Package/Ordering Information	Changed Package Ordering Information table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF102AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		REF102P A	Samples
REF102AU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102AU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102AUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		REF102P B	Samples
REF102BU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U B	Samples
REF102BUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U B	Samples
REF102CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	REF102P C	Samples
REF102CPG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	REF102P C	Samples
REF102CU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples
REF102CU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples
REF102CUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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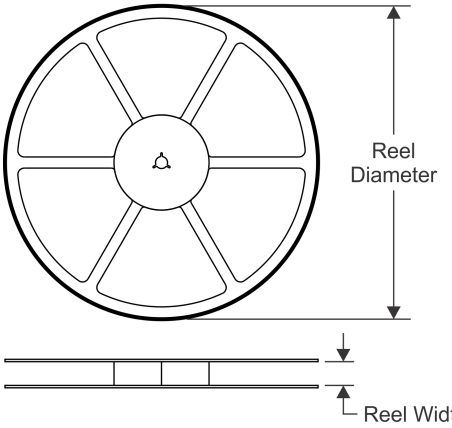
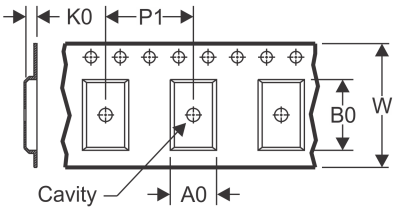
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

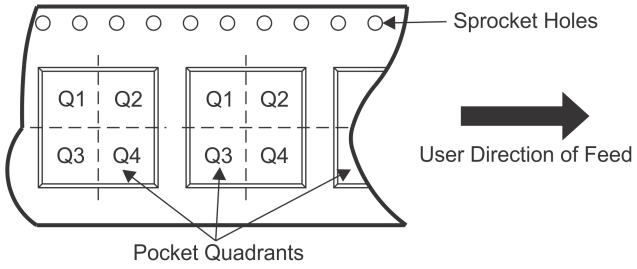


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

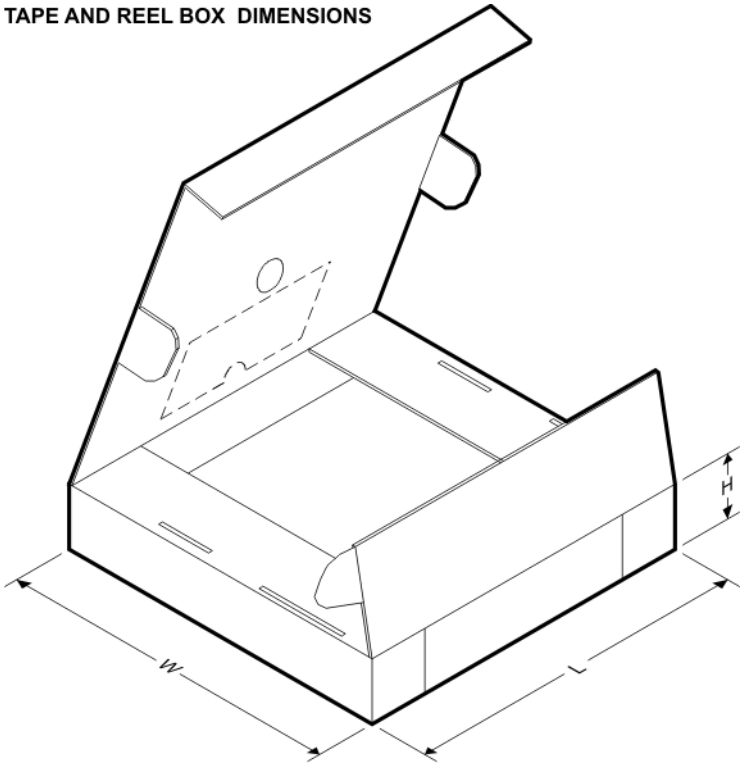
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF102AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF102CU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

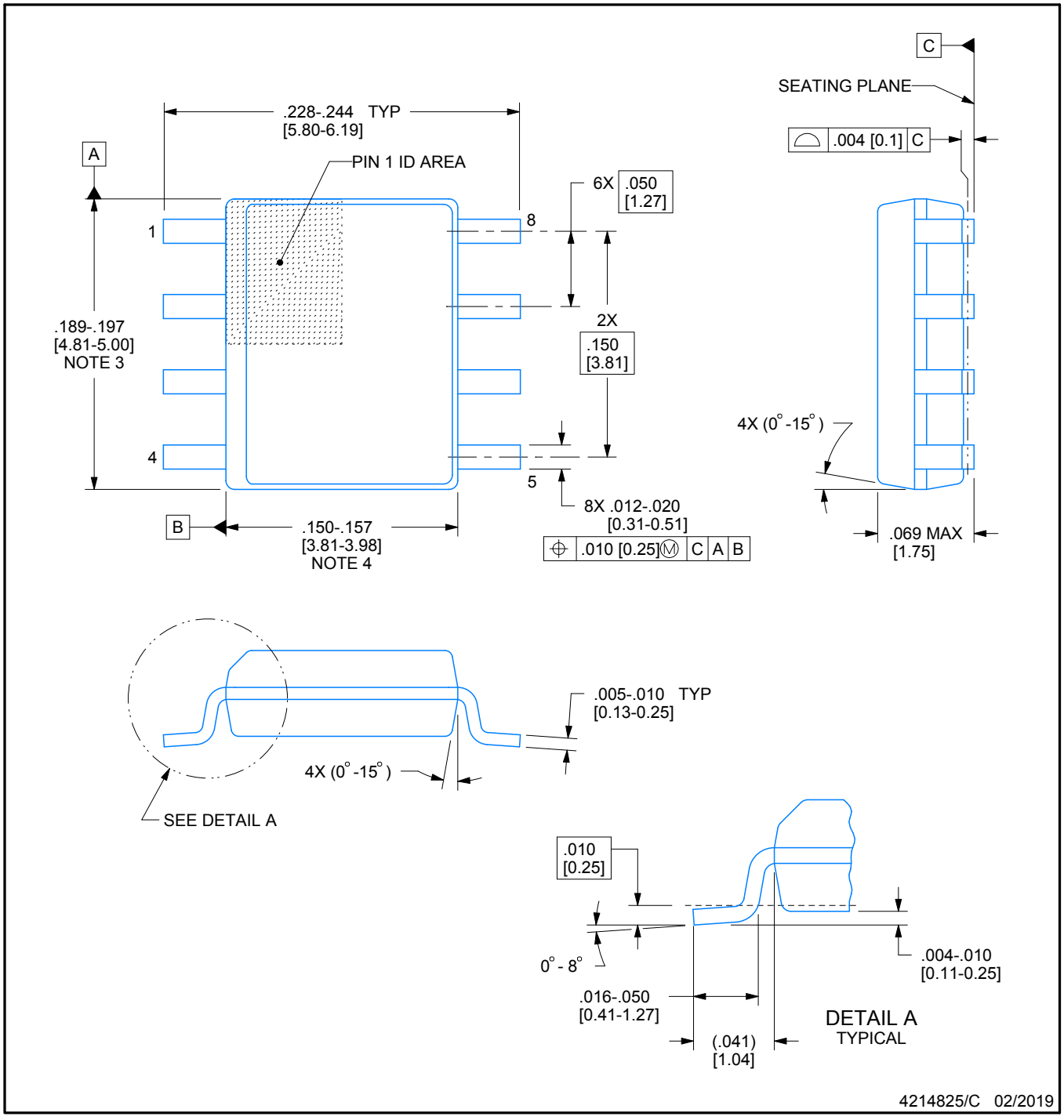
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF102AU/2K5	SOIC	D	8	2500	853.0	449.0	35.0
REF102CU/2K5	SOIC	D	8	2500	853.0	449.0	35.0

PACKAGE OUTLINE

D0008A

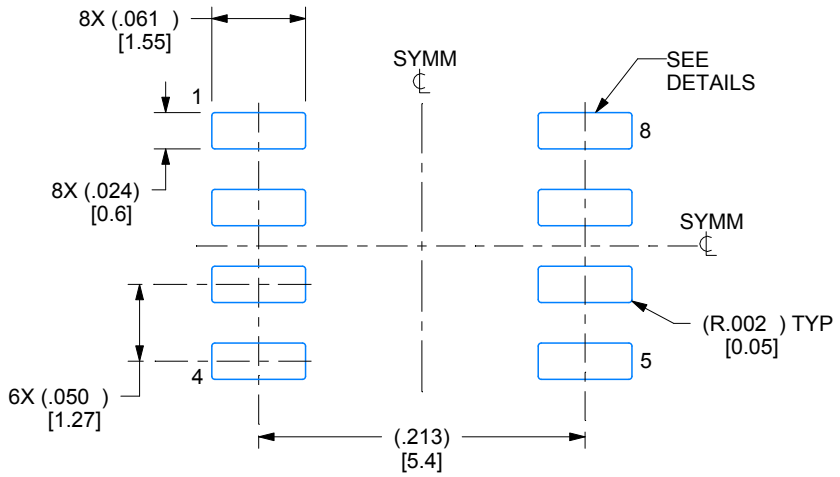
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

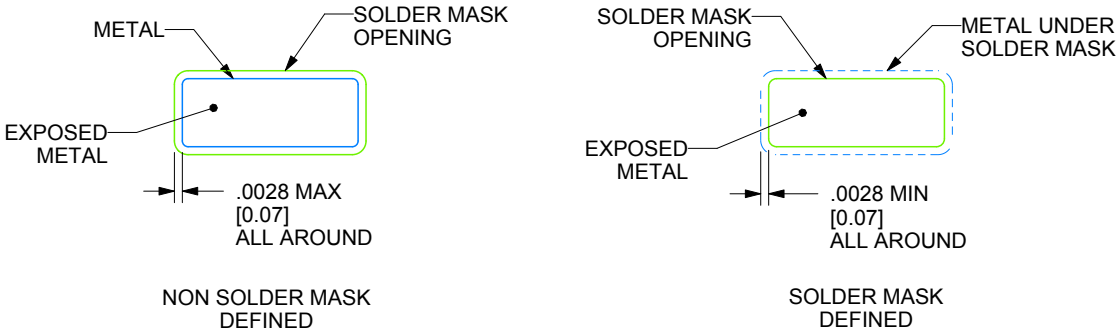


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

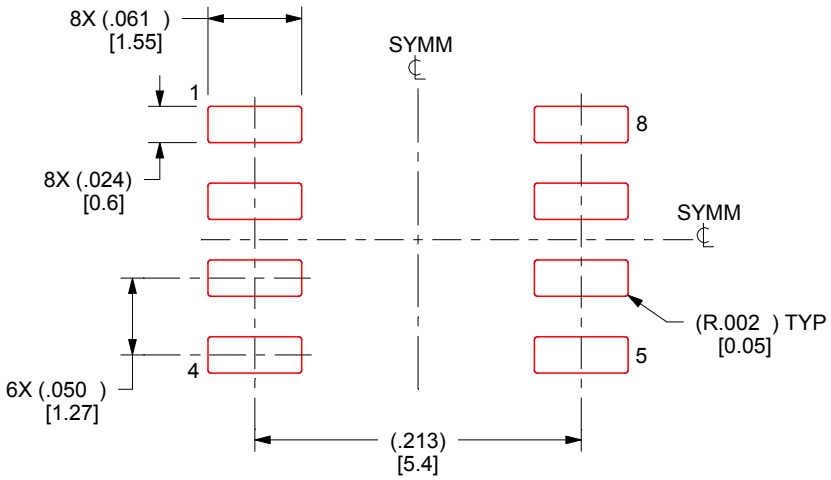


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



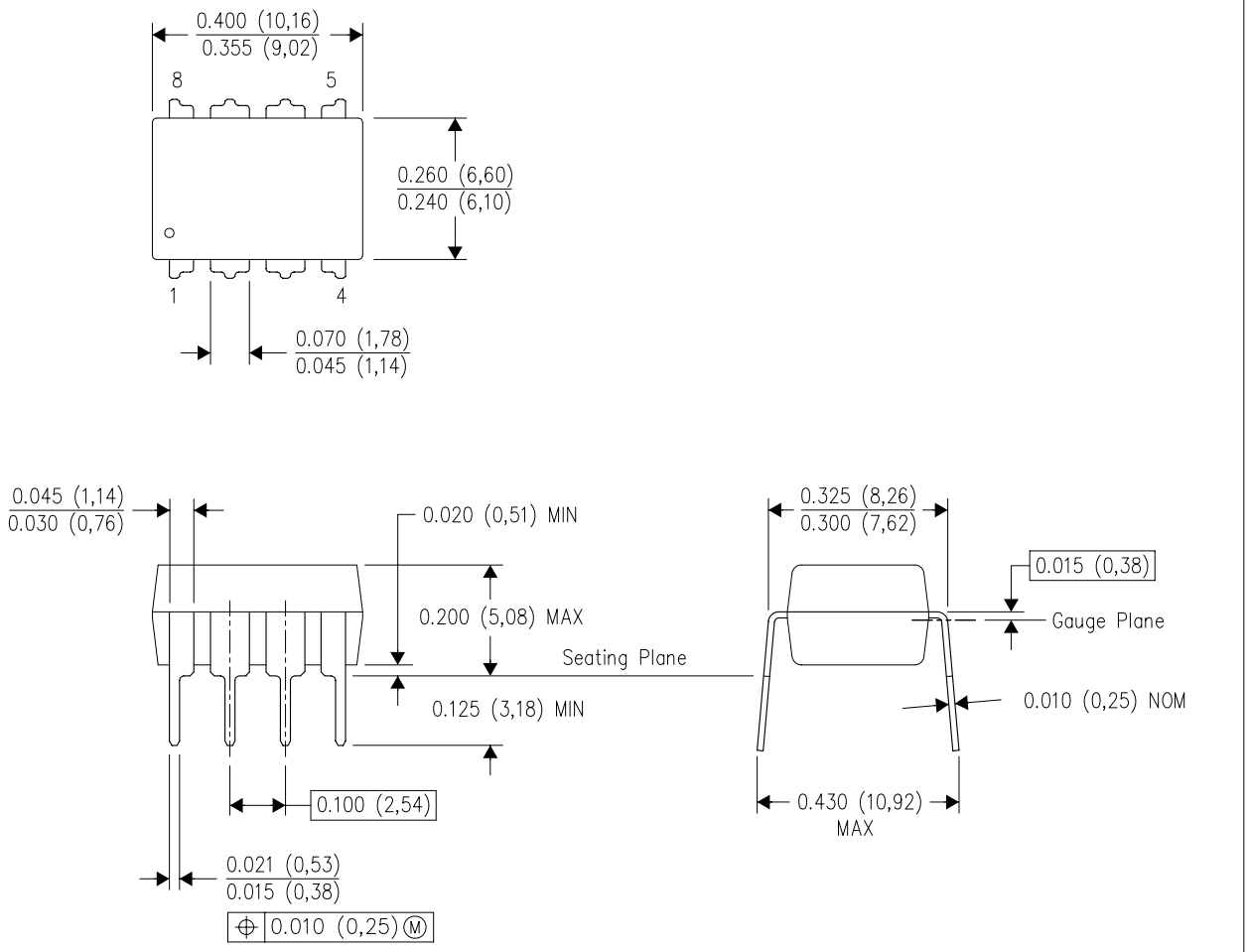
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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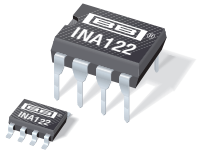
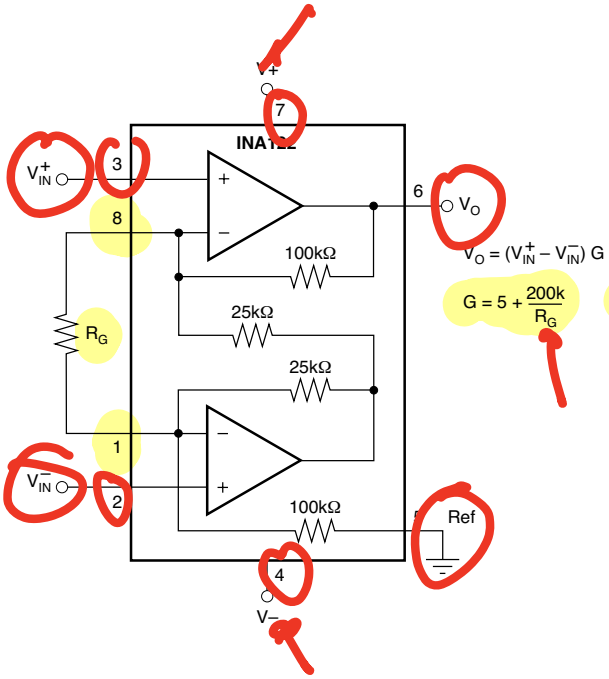


INA122

Single Supply, *Micro*Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 60μA
- WIDE POWER SUPPLY RANGE
  - Single Supply: 2.2V to 36V
  - Dual Supply: –0.9/+1.3V to ±18V
- COMMON-MODE RANGE TO (V–)–0.1V
- RAIL-TO-RAIL OUTPUT SWING
- LOW OFFSET VOLTAGE: 250μV max
- LOW OFFSET DRIFT: 3μV/°C max
- LOW NOISE: 60nV/√Hz
- LOW INPUT BIAS CURRENT: 25nA max
- 8-PIN DIP AND SO-8 SURFACE-MOUNT



APPLICATIONS

- PORTABLE, BATTERY OPERATED SYSTEMS
- INDUSTRIAL SENSOR AMPLIFIER:
  - Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIER:
  - ECG, EEG, EMG
- MULTI-CHANNEL DATA ACQUISITION

DESCRIPTION

The INA122 is a precision instrumentation amplifier for accurate, low noise differential signal acquisition. Its two-op-amp design provides excellent performance with very low quiescent current, and is ideal for portable instrumentation and data acquisition systems.

The INA122 can be operated with single power supplies from 2.2V to 36V and quiescent current is a mere 60μA. It can also be operated from dual supplies. By utilizing an input level-shift network, input common-mode range extends to 0.1V below negative rail (single supply ground).

A single external resistor sets gain from 5V/V to 10000V/V. Laser trimming provides very low offset voltage (250μV max), offset voltage drift (3μV/°C max) and excellent common-mode rejection.

Package options include 8-pin plastic DIP and SO-8 surface-mount packages. Both are specified for the –40°C to +85°C extended industrial temperature range.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1388B
Printed in U.S.A. October, 1997
SBOS069

SPECIFICATIONS

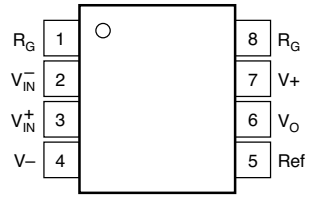
At T_A = +25°C, V_S = +5V, R_L = 20kΩ connected to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	INA122P, U			INA122PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI			±100	±250		±150	±500	µV
vs Temperature			±1	±3		*	±5	µV/°C
vs Power Supply (PSRR)	V_S = +2.2V to +36V		10	30		*	100	µV/V
Input Impedance			10^{10} ll 3			*		Ω ll pF
Safe Input Voltage	R_S = 0	(V–)–0.3		(V+)+0.3	*		*	V
	R_S = 10kΩ	(V–)–40		(V+)+40	*		*	V
Common-Mode Voltage Range		0		3.4	*		*	V
Common-Mode Rejection	V_{CM} = 0V to 3.4V	83	96		76	90		dB
INPUT BIAS CURRENT			–10	–25		*	–50	nA
vs Temperature			±40			*		pA/°C
Offset Current			±1	±2		*	±5	nA
vs Temperature			±40			*		pA/°C
GAIN			G = 5 to 10k			*		V/V
Gain Equation			G = 5 + 200kΩ/R_G			*		V/V
Gain Error	G = 5		±0.05	±0.1		*	±0.15	%
vs Temperature	G = 5		5	10		*	*	ppm/°C
Gain Error	G = 100		±0.3	±0.5		*	±1	%
vs Temperature	G = 100		±25	±100		*	*	ppm/°C
Nonlinearity	G = 100, V_O = –14.85V to +14.9V		±0.005	±0.012		*	±0.024	%
NOISE (RTI)								
Voltage Noise, f = 1kHz			60			*		nV/√Hz
f = 100Hz			100			*		nV/√Hz
f = 10Hz			110			*		nV/√Hz
f_B = 0.1Hz to 10Hz			2			*		µVp-p
Current Noise, f = 1kHz			80			*		fA/√Hz
f_B = 0.1Hz to 10Hz			2			*		pAp-p
OUTPUT								
Voltage, Positive	V_S = ±15V	(V+)–0.1	(V+)–0.05		*	*		V
Negative	V_S = ±15V	(V–)+0.15	(V–)+0.1		*	*		V
Short-Circuit Current	Short-Circuit to Ground		+3/–30			*		mA
Capacitive Load Drive			1			*		nF
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 5		120			*		kHz
	G = 100		5			*		kHz
	G = 500		0.9			*		kHz
Slew Rate			+0.08/–0.16			*		V/µs
Settling Time, 0.01%	G = 5		350			*		µs
	G = 100		450			*		µs
	G = 500		1.8			*		ms
Overload Recovery	50% Input Overload		3			*		µs
POWER SUPPLY								
Voltage Range, Single Supply		+2.2	+5	+36	*	*	*	V
Dual Supplies		–0.9/+1.3		±18	*	*	*	V
Current	I_O = 0		60	85		*	*	µA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operation		–55		+85	*		*	°C
Storage		–55		+125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Pin DIP			150			*		°C/W
SO-8 Surface-Mount			150			*		°C/W

* Specification same as INA122P, INA122U.

PIN CONFIGURATION

Top View **8-Pin DIP, SO-8**



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Signal Input Terminals, Voltage[2]	(V–)–0.3V to (V+)+0.3V
Current[2]	5mA
Output Short Circuit	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are internally diode-clamped to the power supply rails. Input signals that can exceed the supply rails by more than 0.3V should be current-limited to 5mA or less.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
INA122PA	8-Pin DIP	006
INA122P	8-Pin DIP	006
INA122UA	SO-8 Surface Mount	182
INA122U	SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

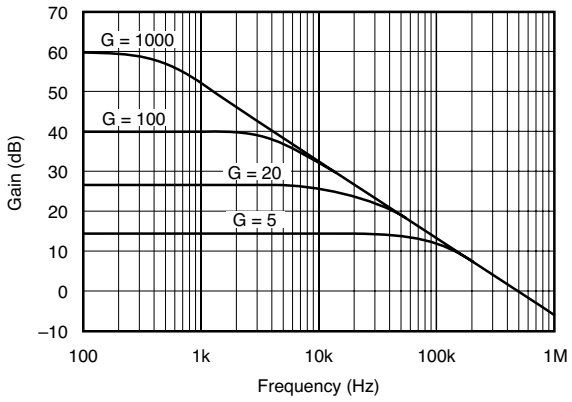
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

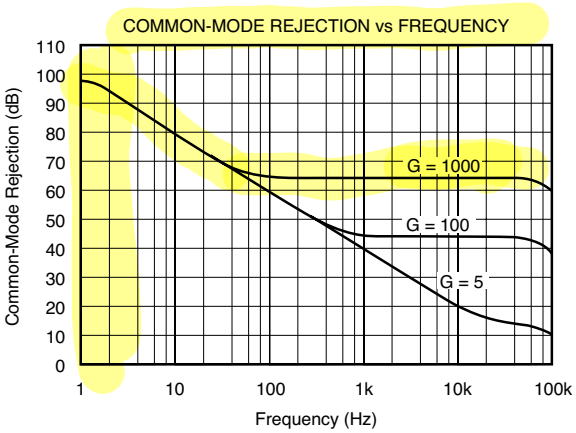
TYPICAL PERFORMANCE CURVES

At T_A = +25°C and V_S = ±5V, unless otherwise noted.

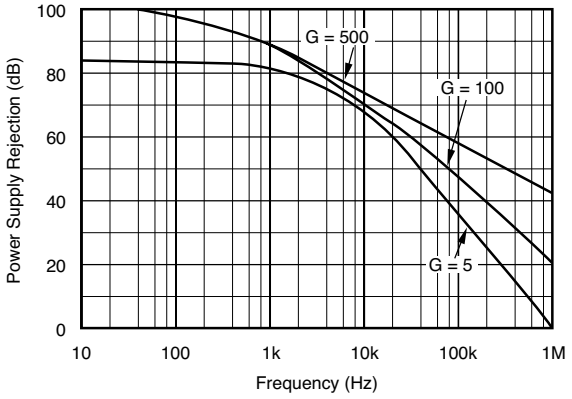
GAIN vs FREQUENCY



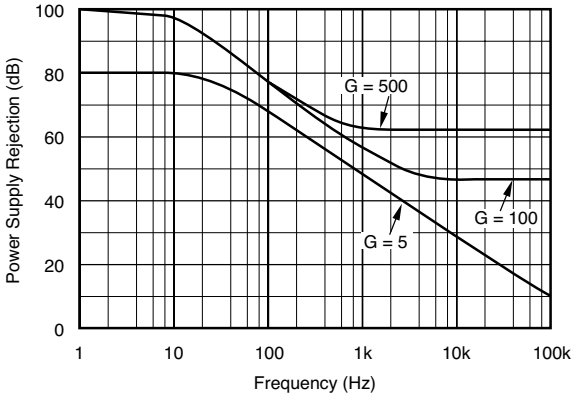
COMMON-MODE REJECTION vs FREQUENCY



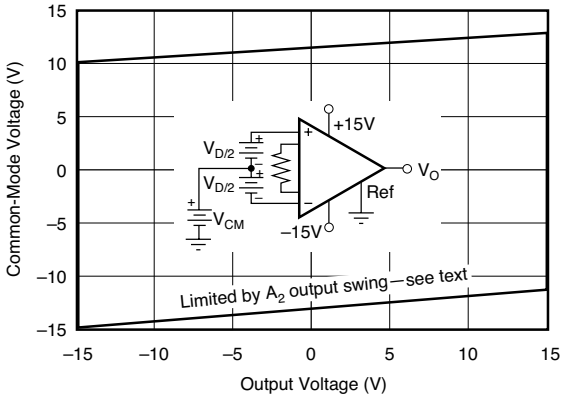
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



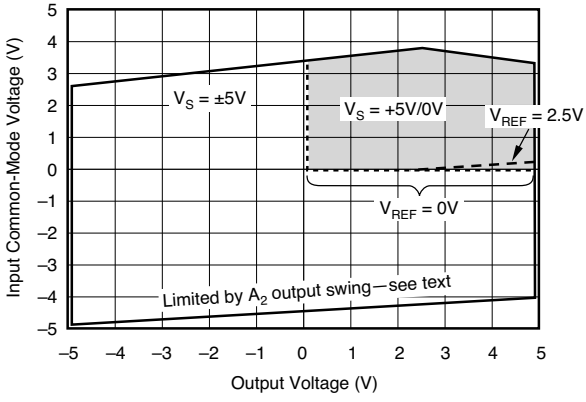
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, V_S = ±15V, G = 5



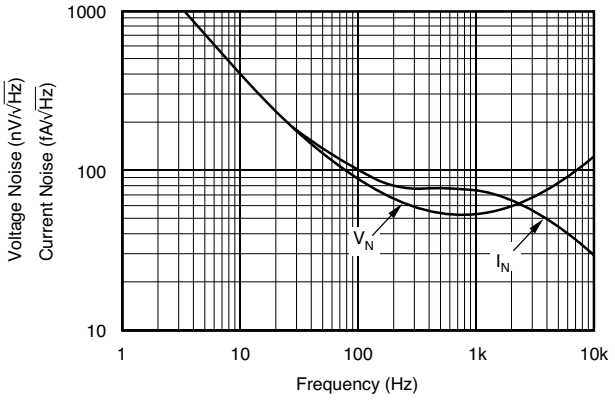
INPUT COMMON-MODE VOLTAGE vs OUTPUT VOLTAGE, V_S = ±5V, G = 5



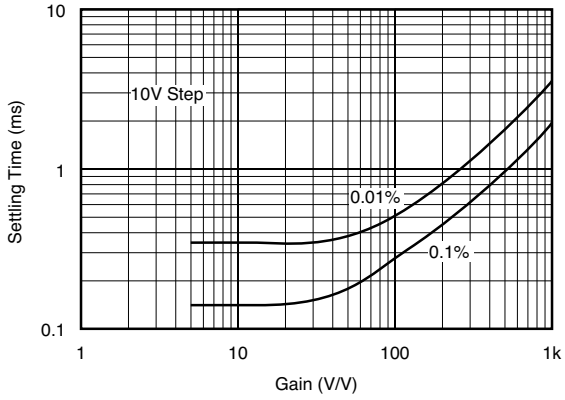
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C and V_S = ±5V, unless otherwise noted.

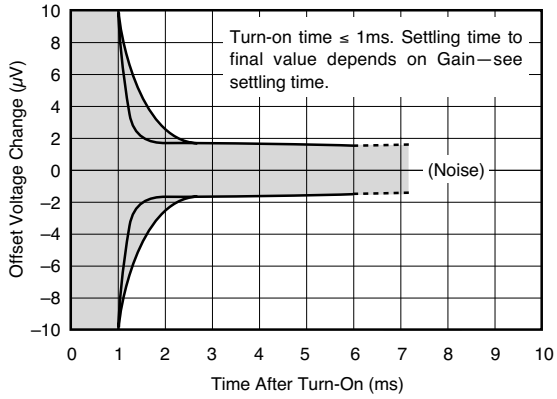
VOLTAGE and CURRENT NOISE DENSITY vs FREQUENCY (RTI)



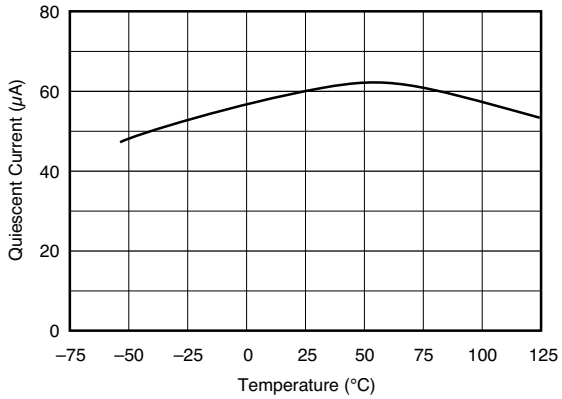
SETTLING TIME vs GAIN



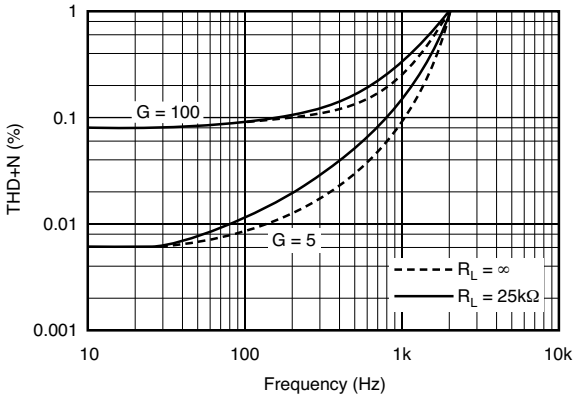
INPUT-REFERRED OFFSET VOLTAGE WARM-UP



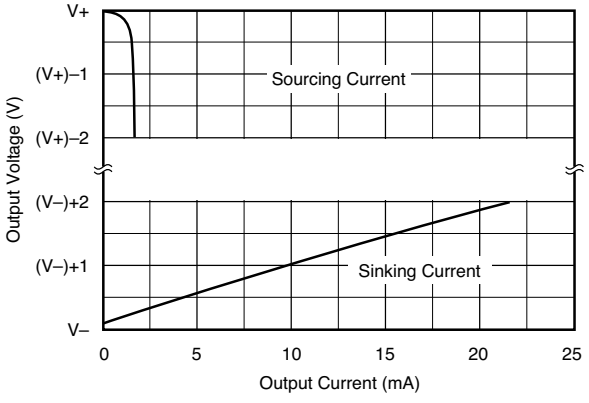
QUIESCENT CURRENT vs TEMPERATURE



TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



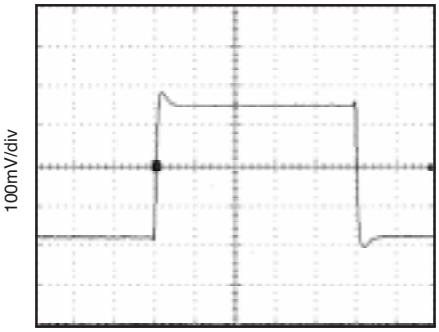
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



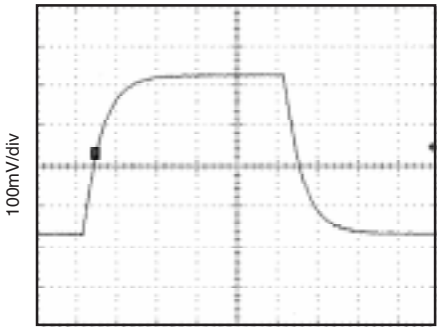
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C and V_S = ±5V, unless otherwise noted.

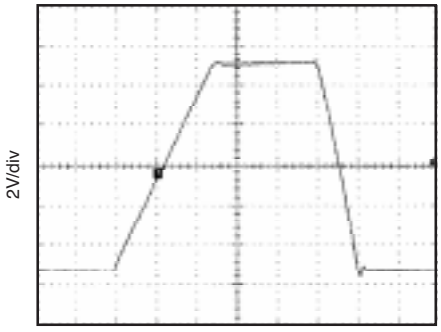
SMALL-SIGNAL STEP RESPONSE
G = 5



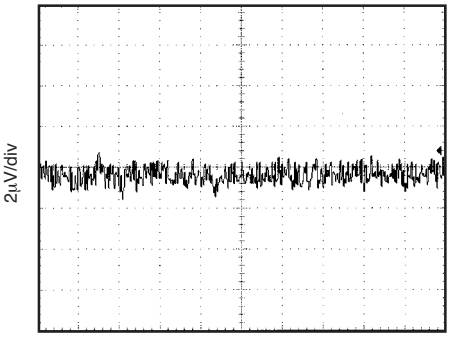
SMALL-SIGNAL STEP RESPONSE
G = 100



LARGE-SIGNAL STEP RESPONSE
G = 5



INPUT-REFERRED NOISE VOLTAGE
0.1Hz to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA122. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to ensure good common-mode rejection. A resistance of 10Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR.

SETTING THE GAIN

Gain of the INA122 is set by connecting a single external resistor, R_G, as shown:

$$G = 5 + \frac{200k\Omega}{R_G} \quad (1)$$

Commonly used gains and R_G resistor values are shown in Figure 1.

The 200kΩ term in equation 1 comes from the internal metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA122.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1).

OFFSET TRIMMING

The INA122 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.

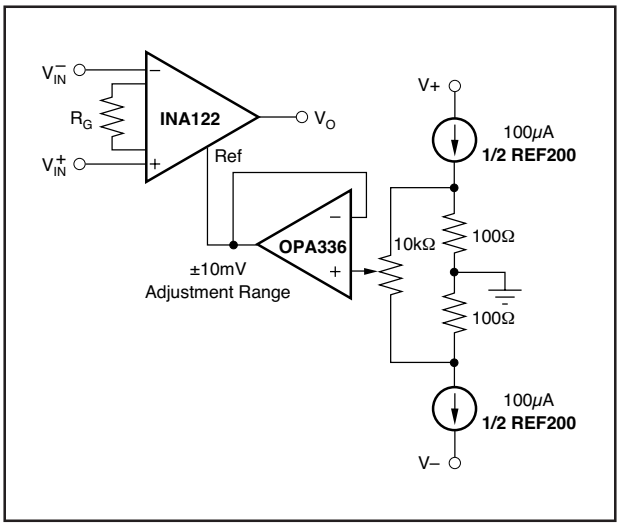


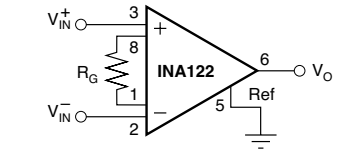
FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA122 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately –10nA (current flows out of the input terminals). High input impedance means that this input bias current changes very little with varying input voltage.

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G VALUE
5	NC	NC
10	40k	40.2k
20	13.33k	13.3k
50	4444	4420
100	2105	2100
200	1026	1020
500	404	402
1000	201	200
2000	100.3	100
5000	40	40.2
10000	20	20

NC: No Connection.



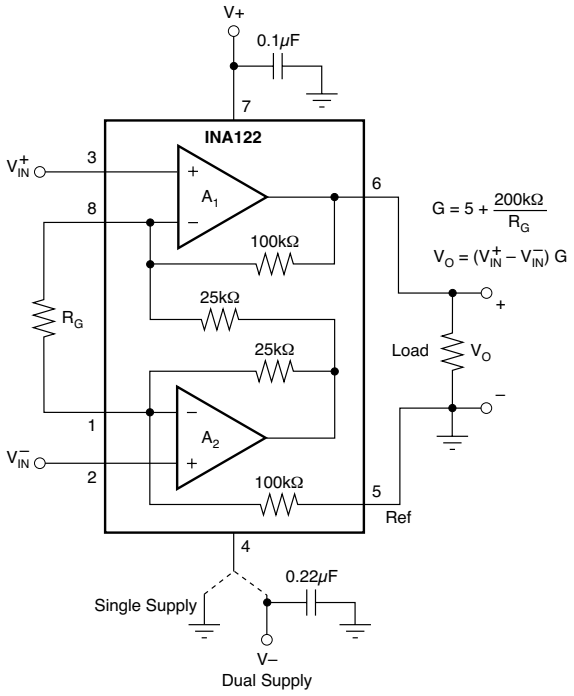


FIGURE 1. Basic Connections.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA122 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

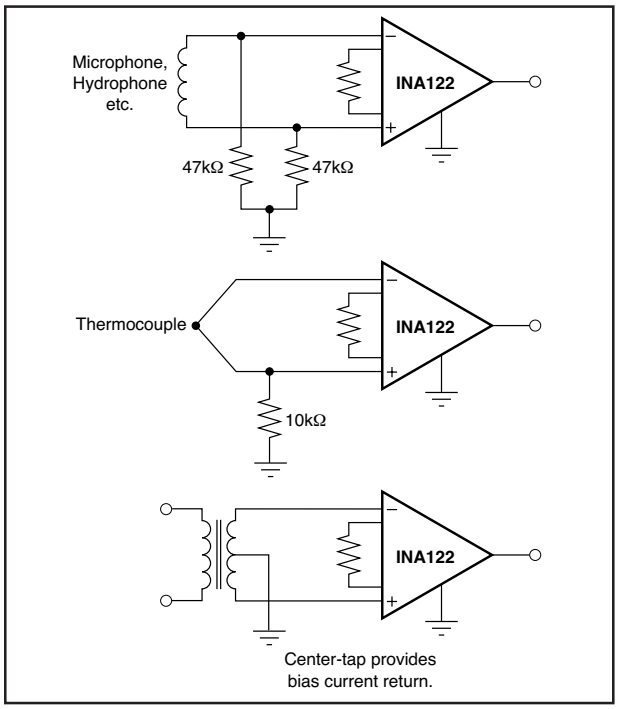


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT PROTECTION

The inputs of the INA122 are protected with internal diodes connected to the power supply rails (Figure 4). These diodes will clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.3V, the input signal current should be limited to less than 5mA to protect the internal clamp diodes. This can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

INPUT COMMON-MODE RANGE

The common-mode range for some common operating conditions is shown in the typical performance curves. The INA122 can operate over a wide range of power supply and V_{REF} configurations, making it impractical to provide a comprehensive guide to common-mode range limits for all possible conditions. The most commonly overlooked overload condition occurs by attempting to exceed the output swing of A_2, an internal circuit node that cannot be measured. Calculating the expected voltages at A_2's output (see equation in Figure 4) provides a check for the most common overload conditions.

The design of A_1 and A_2 are identical and their outputs can swing to within approximately 100mV of the power supply rails, depending on load conditions. When A_2's output is saturated, A_1 can still be in linear operation, responding to changes in the non-inverting input voltage. This may give the appearance of linear operation but the output voltage is invalid.

A single supply instrumentation amplifier has special design considerations. Using commonly available single-supply op amps to implement the two-op amp topology will not yield equivalent performance. For example, consider the condition where both inputs of common single-supply op amps are

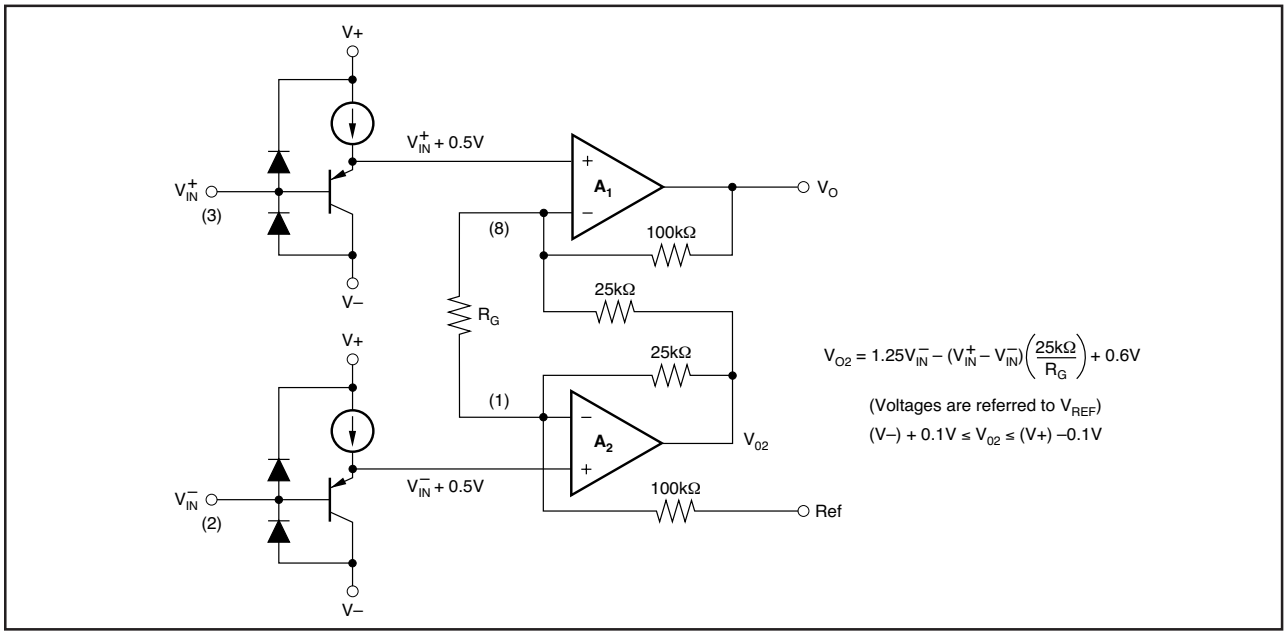


FIGURE 4. INA122 Simplified Circuit Diagram.

equal to 0V. The outputs of both A_1 and A_2 must be 0V. But any small positive voltage applied to V_{IN}^+ requires that A_2's output must swing below 0V, which is clearly impossible without a negative power supply.

To achieve common-mode range that extends to single-supply ground, the INA122 uses precision level-shifting buffers on its inputs. This shifts both inputs by approximately +0.5V, and through the feedback network, shifts A_2's output by approximately +0.6V. With both inputs and V_{REF} at single-supply, A_2's output is well within its linear range. A positive V_{IN}^+ causes A_2's output to swing below 0.6V.

As a result of this input level-shifting, the voltages at pin 1 and pin 8 are not equal to their respective input terminal voltages (pins 2 and 3). For most applications, this is not important since only the gain-setting resistor connects to these pins.

LOW VOLTAGE OPERATION

The INA122 can be operated on a single power supply as low as +2.2V (or a total of +2.2V on dual supplies). Performance remains excellent throughout the power supply range up to +36V (or ±18V). Most parameters vary only slightly throughout this supply voltage range—see typical performance curves.

Operation at very low supply voltage requires careful attention to ensure that the common-mode voltage remains within its linear range.

LOW QUIESCENT CURRENT OPERATION

The INA122 maintains its low quiescent current (60µA) while the output is within linear operation (up to 200mV from the supply rails). When the input creates a condition that overdrives the output into saturation, quiescent current increases. With V_O overdriven into the positive rail, the quiescent current increases to approximately 400µA. Likewise, with V_O overdriven into the negative rail (single supply ground) the quiescent current increases to approximately 200µA.

OUTPUT CURRENT RANGE

Output sourcing and sinking current values versus the output voltage ranges are shown in the typical performance curves. The positive and negative current limits are not equal. Positive output current sourcing will drive moderate to high load impedances. Battery operation normally requires the careful management of power consumption to keep load impedances very high throughout the design.

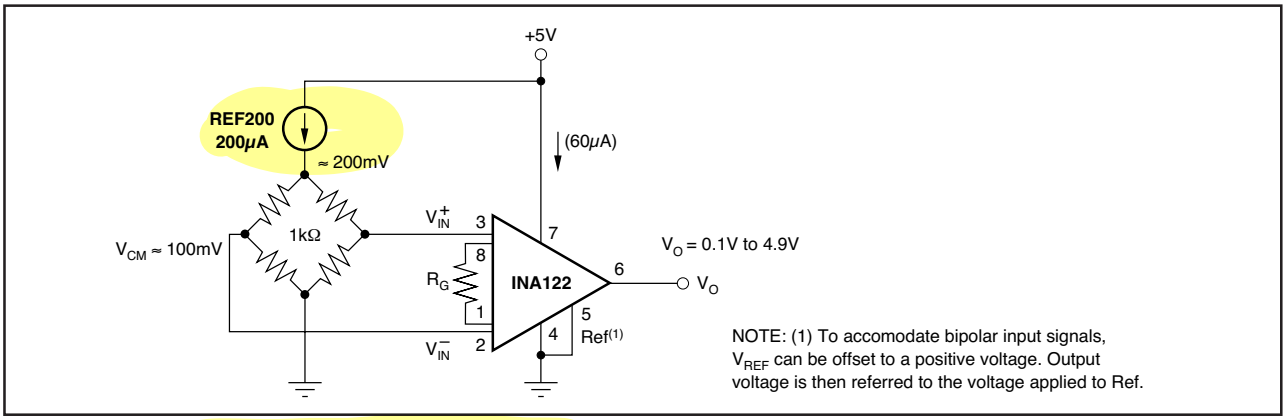


FIGURE 5. Micropower Single Supply Bridge Amplifier.

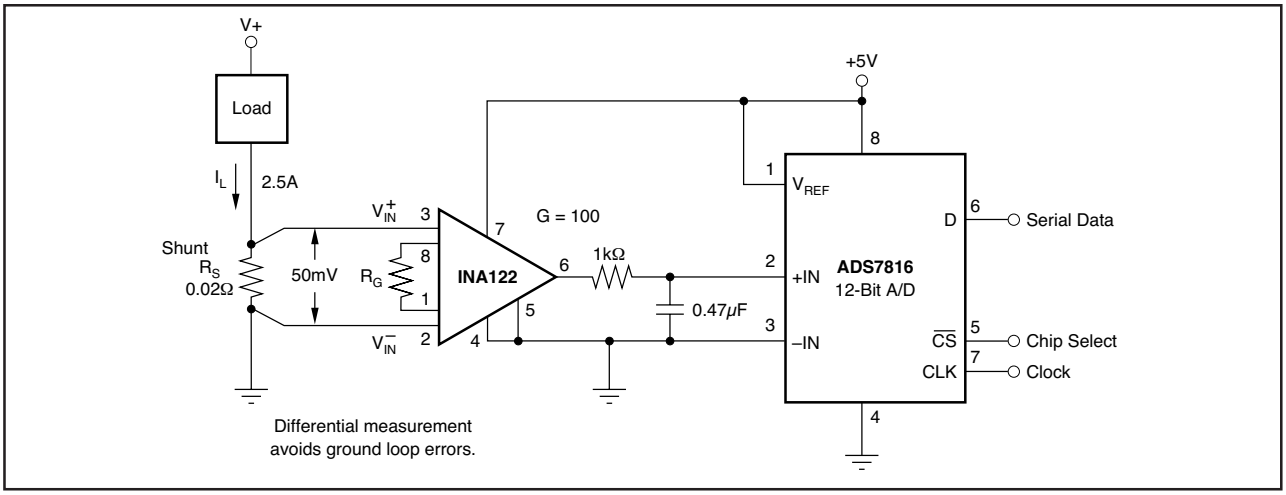


FIGURE 6. Single-Supply Current Shunt Measurement.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA122P	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	INA122P	
INA122PA	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA122P A	
INA122PAG4	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA122P A	
INA122U	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U	
INA122U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U	Samples
INA122UA	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U A	
INA122UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

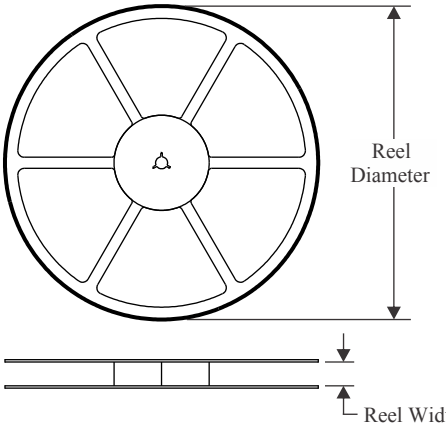
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

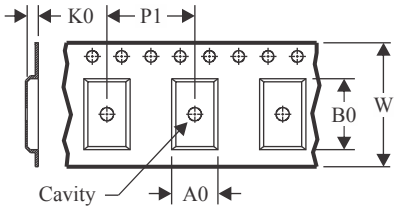
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

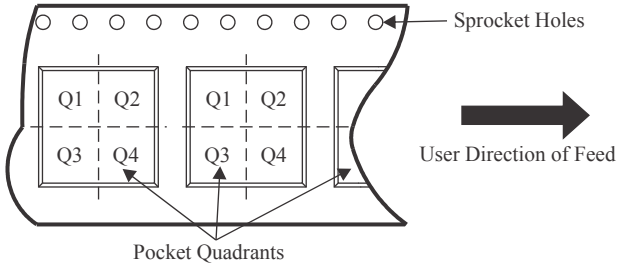


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

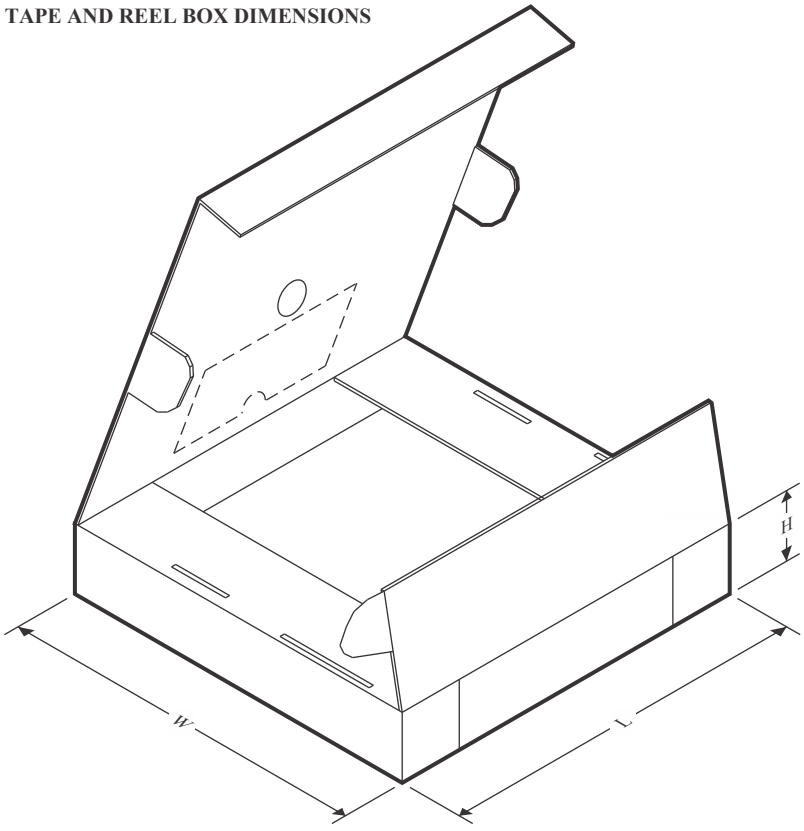
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA122U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA122UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

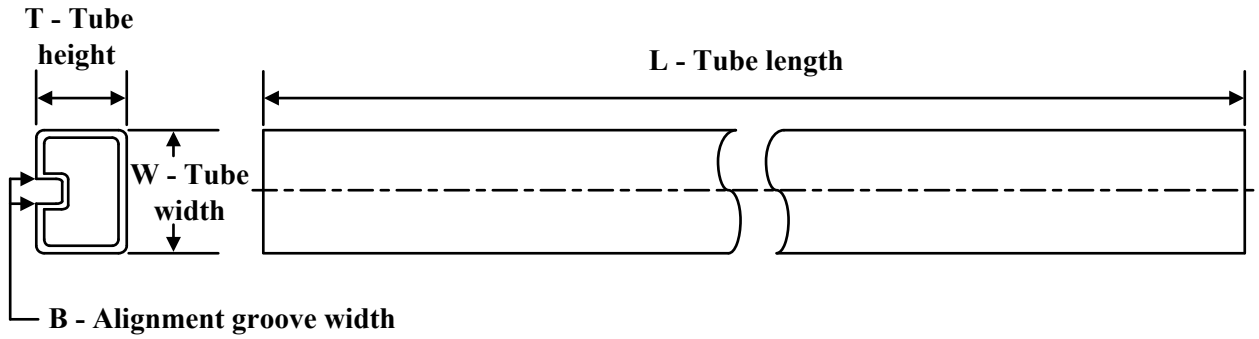
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA122U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA122UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA122P	P	PDIP	8	50	506	13.97	11230	4.32
INA122PA	P	PDIP	8	50	506	13.97	11230	4.32
INA122PAG4	P	PDIP	8	50	506	13.97	11230	4.32
INA122U	D	SOIC	8	75	506.6	8	3940	4.32
INA122UA	D	SOIC	8	75	506.6	8	3940	4.32

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