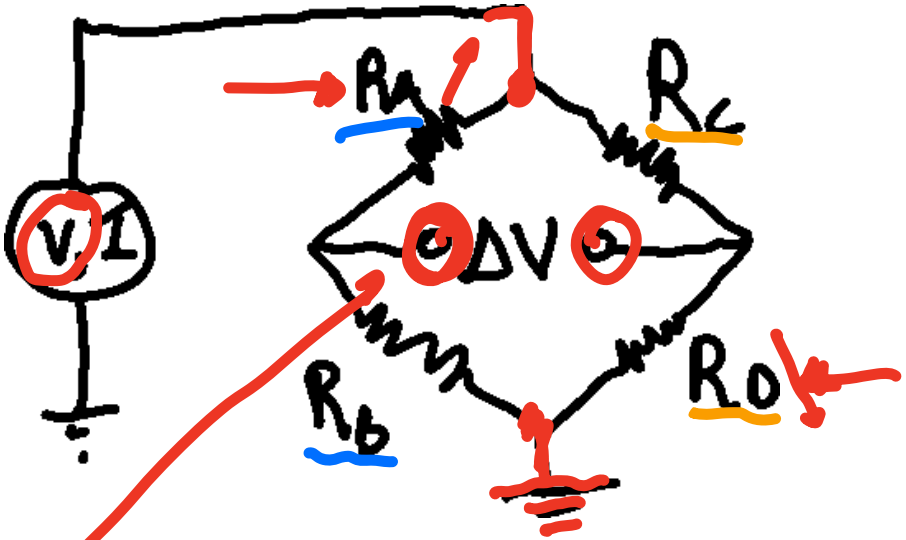
Instrumentation amplifiers, load-cell amplification

The Wheatstone bridge



Suppose we have a constant V bridge excitation. Then the total current passing through the bridge is:

$$V_B = (R_A + R_B) \| (R_C + R_D)\, I$$

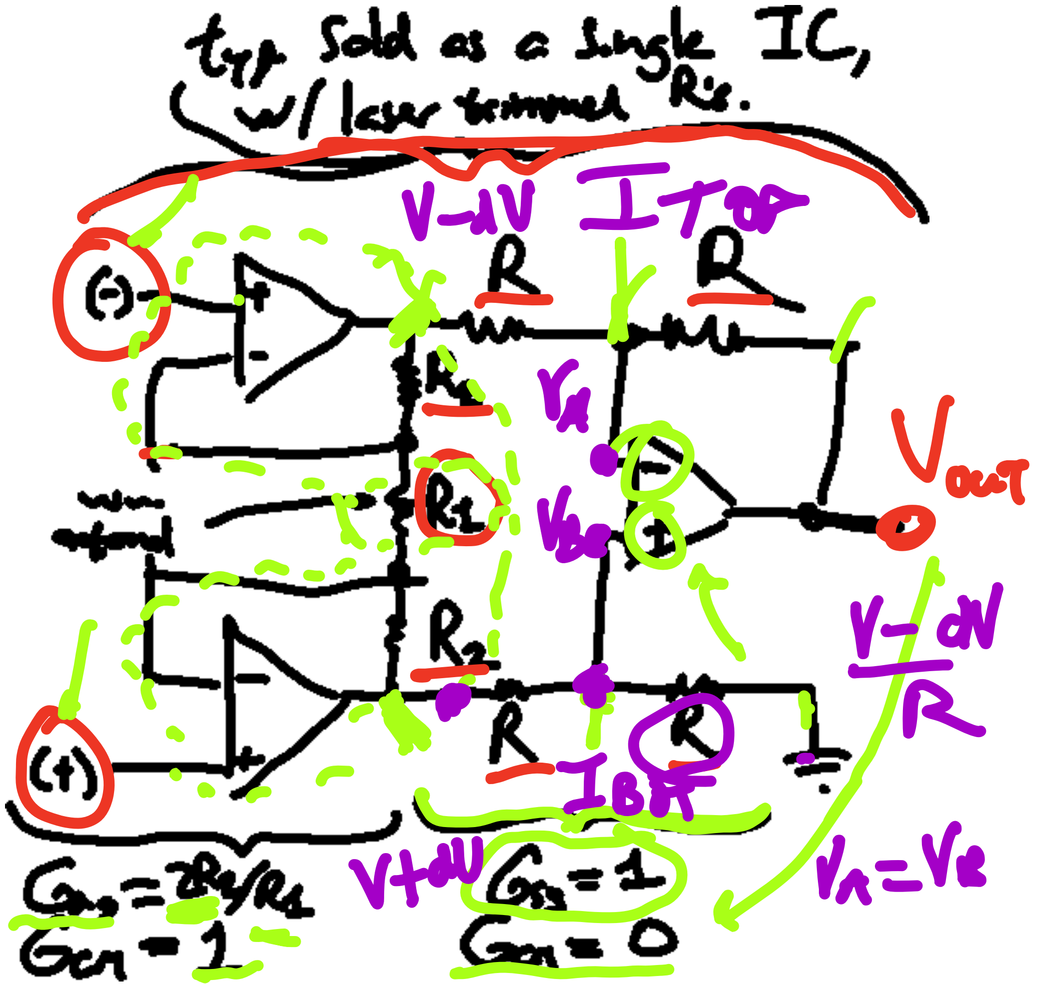
For simplicity, and to get an idea of how this bridge works, let's assume that both dividers have an equal resistance, and furthermore that all resister values are identical. Then $\Delta V = 0$.

Now, consider a case where R_A increases by an amount dR, and R_D decreases by dR.
In this case, the current passing through the two halves of the bridge (each a divider!) is no longer identical. In fact, the left current is: $V/(R_A + dR + R_B)$, while the right current is $V/(R_C + R_D - dR)$.

Thus, the voltage on the left is $R_B * V / (R_A + dR + R_B)$, and on the right, $(R_D - dR)*V/(R_C + R_D - dR)$, and after a significant amount of algebra, we find to leading order that $\Delta V \sim 2\, dR$ (the exact calculation you can do if you like!)

Fundamentally, this circuit becomes ***non-linear*** when dR becomes large compared with all the R in the bridge.

Often we are tasked with the measurement of a transducer's output



The main challenge addressed by instrumentation amplifiers is *high rejection of common-mode voltage (CMRR)*

The high CMRR is necessary because often transducers (such as load cells) have high common-mode signals (of order several V), while the signal of interest is a differential signal in the mV-scale.

If we want a 0.1% accuracy of a mV signal, say, then we must reject 5 V-common-mode down to the microvolt level (!) this corresponds to a rejection of over a million times the common-mode!

How can we achieve this?

$$\frac{V_{out}+V_A}{R} = \frac{V+dV}{R} \qquad \frac{V_B = V-dV}{R} = \frac{V_A}{R}$$

$$V_{out} = V+dV-V_A = V+dV-(V-dV)$$

$$= V+dV-V+dV$$

$$= 2dV$$

$$V_{out}-V_A = V_A-(V-dV)$$

$$V_{out} = 2V_A-(V-dV)$$

$$V+dV-V_B = V_B$$

$$V+dV = 2V_B = 2V_A$$

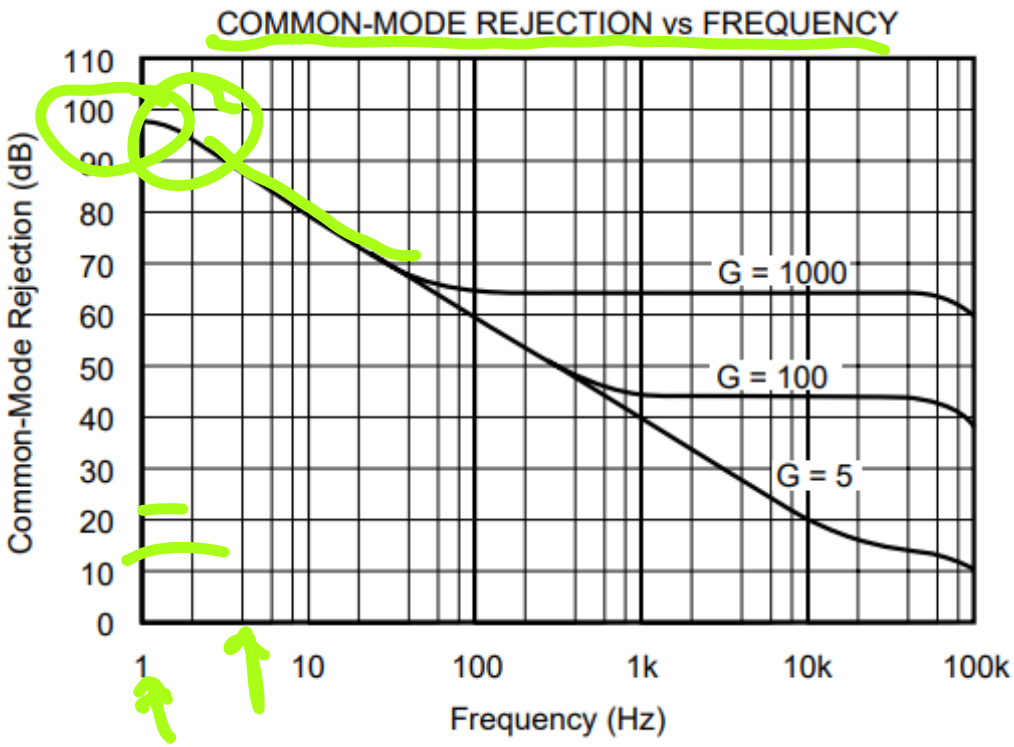
$$V_{out} = V+dV-V+dV = 2dV \checkmark$$

The previous circuit should look familiar from the handout on instrumentation amplifiers.

These are useful devices for discarding common-mode signals!

A word of caution on CMRR in INAs: see from the INA 122 datasheet:

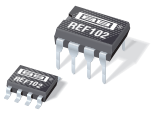
CMRR drops at high-frequency!



Precision Voltage sources: REF 102

High CMRR: ~~INA 122~~

LT 1102



SBVS022B – SEPTEMBER 2000 – REVISED JUNE 2009

10V Precision Voltage Reference

FEATURES

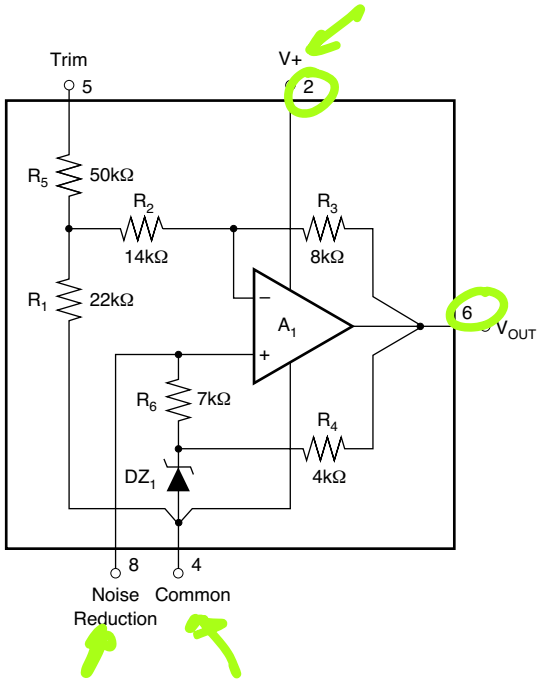
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μV_{PP} typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: PLASTIC DIP, SO-8

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETER
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max C-grade over the industrial temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single-supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.



ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage	+40V
Operating Temperature	
P, U	–25°C to +85°C
Storage Temperature Range	
P, U	–40°C to +125°C
Short-Circuit Protection to Common or V+	Continuous

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

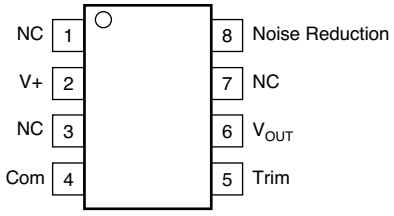
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAX INITIAL ERROR (mV)	MAX DRIFT (PPM/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
REF102AU	±10	±10	SO-8	D	REF102AU
REF102AP	±10	±10	DIP-8	P	REF102AP
REF102BU	±5	±5	SO-8	D	REF102BU
REF102BP	±5	±5	DIP-8	P	REF102BP
REF102CU	±2.5	±2.5	SO-8	D	REF102CU
REF102CP	±2.5	±2.5	DIP-8	P	REF102CP

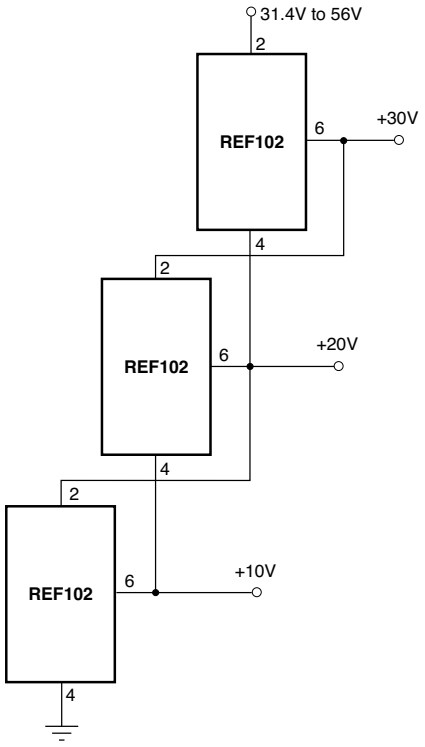
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

Top View **DIP, SO**



NC = Not Connected



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26, where *n* is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

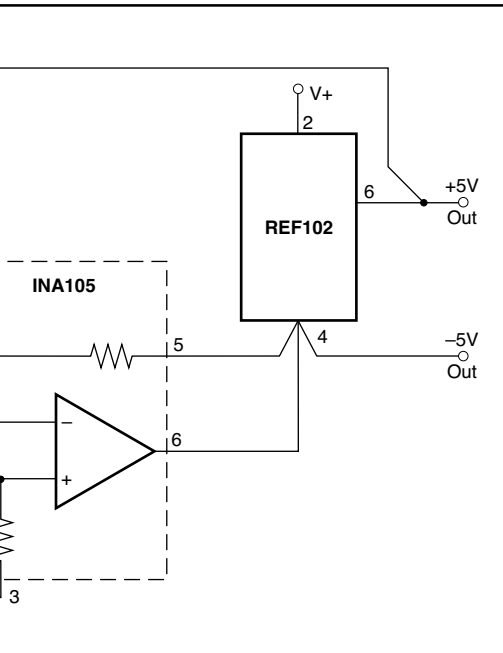


FIGURE 12. ±5V Reference.

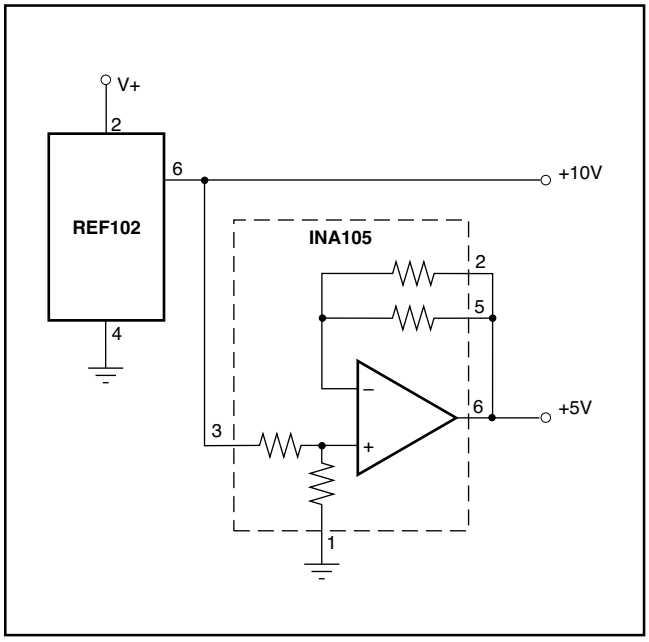


FIGURE 13. +5V and +10V Reference.

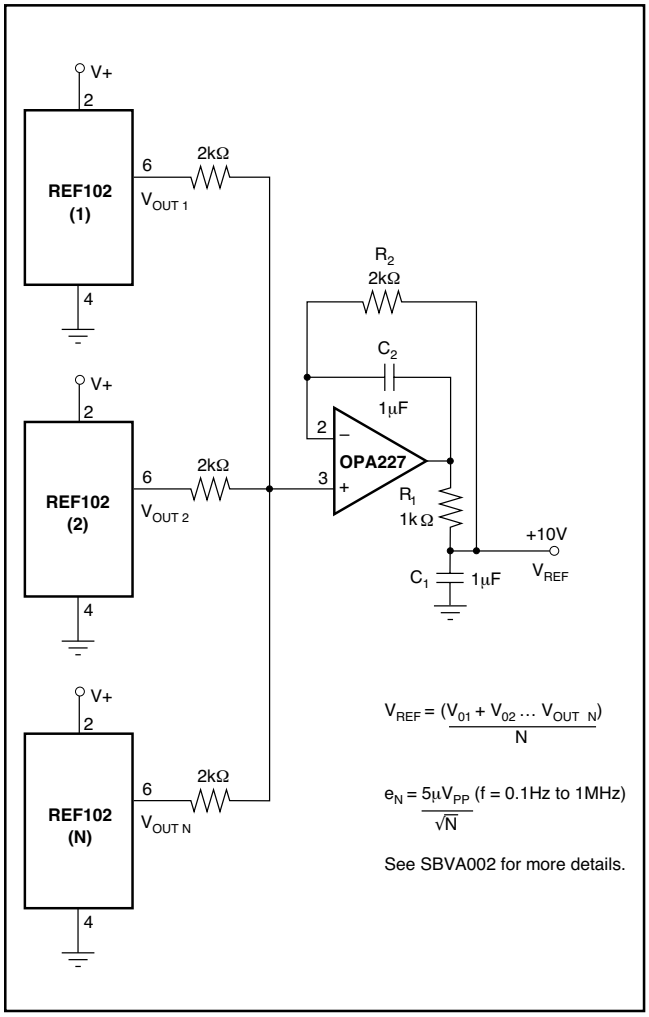


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
6/09	B	2	Absolute Maximum Ratings	Deleted lead temperature rating.
			Package/Ordering Information	Changed Package Ordering Information table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF102AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		REF102P A	Samples
REF102AU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102AU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102AUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		REF102P B	Samples
REF102BU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U B	Samples
REF102BUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U B	Samples
REF102CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	REF102P C	Samples
REF102CPG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	REF102P C	Samples
REF102CU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples
REF102CU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples
REF102CUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

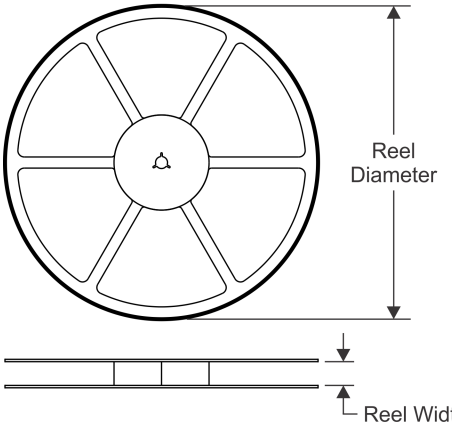
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

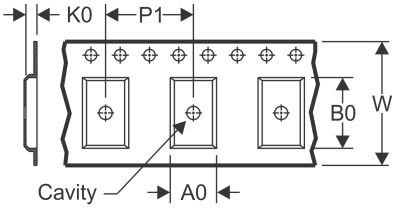
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

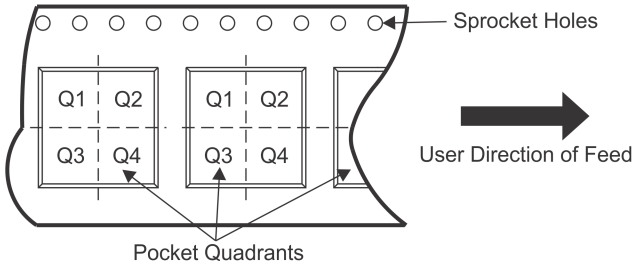


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

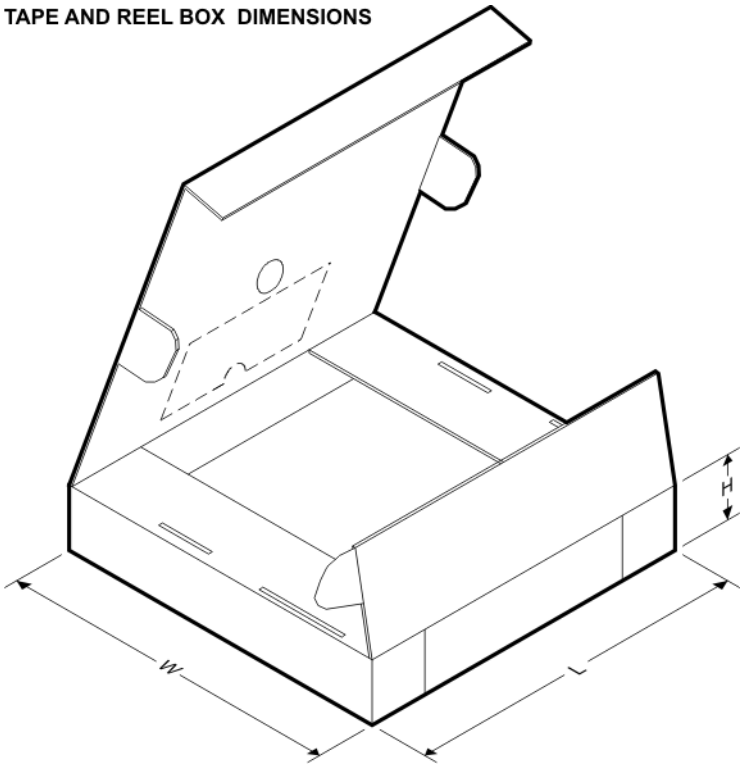
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF102AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF102CU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

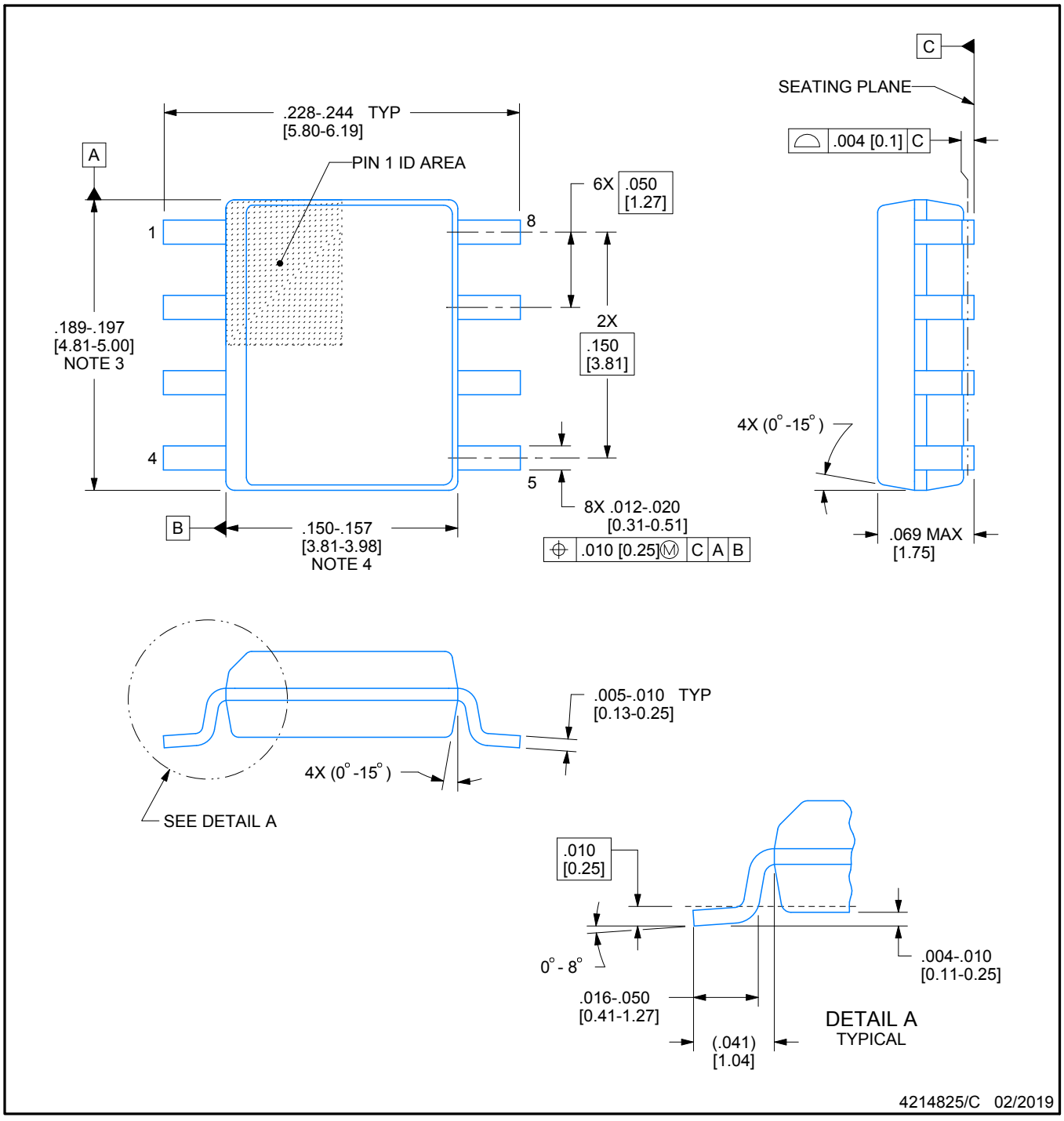
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF102AU/2K5	SOIC	D	8	2500	853.0	449.0	35.0
REF102CU/2K5	SOIC	D	8	2500	853.0	449.0	35.0

PACKAGE OUTLINE

D0008A

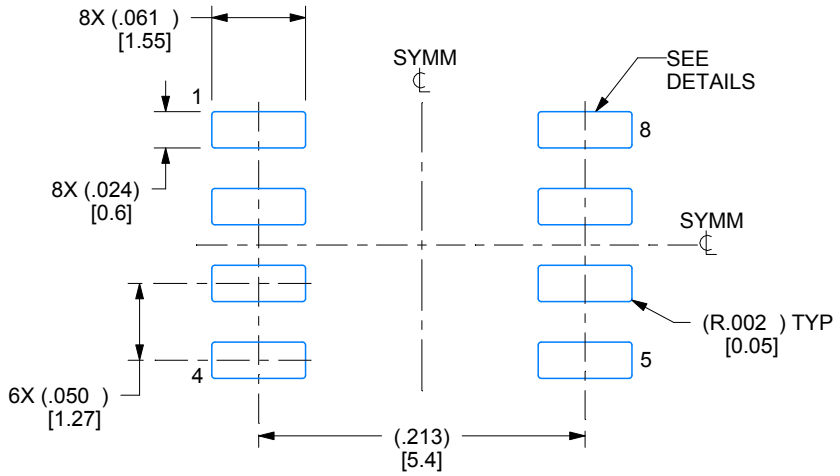
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

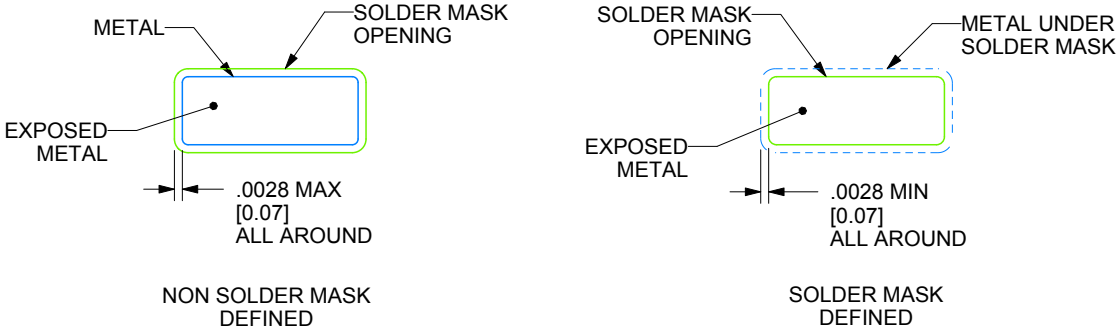


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

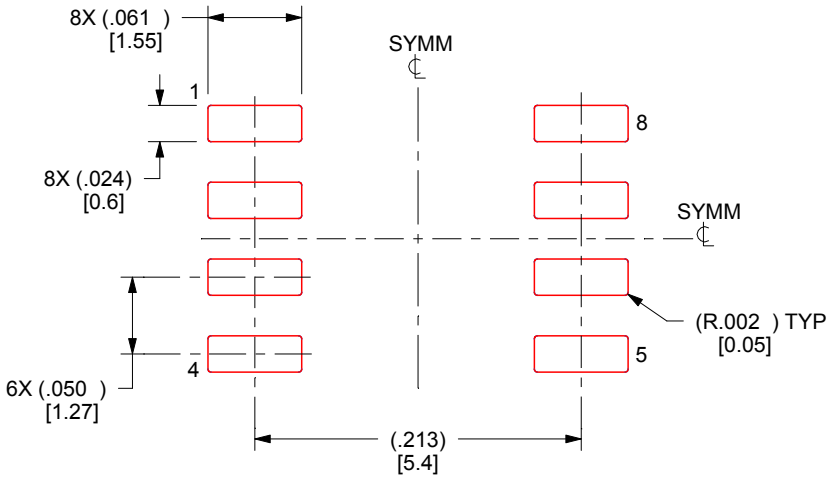
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



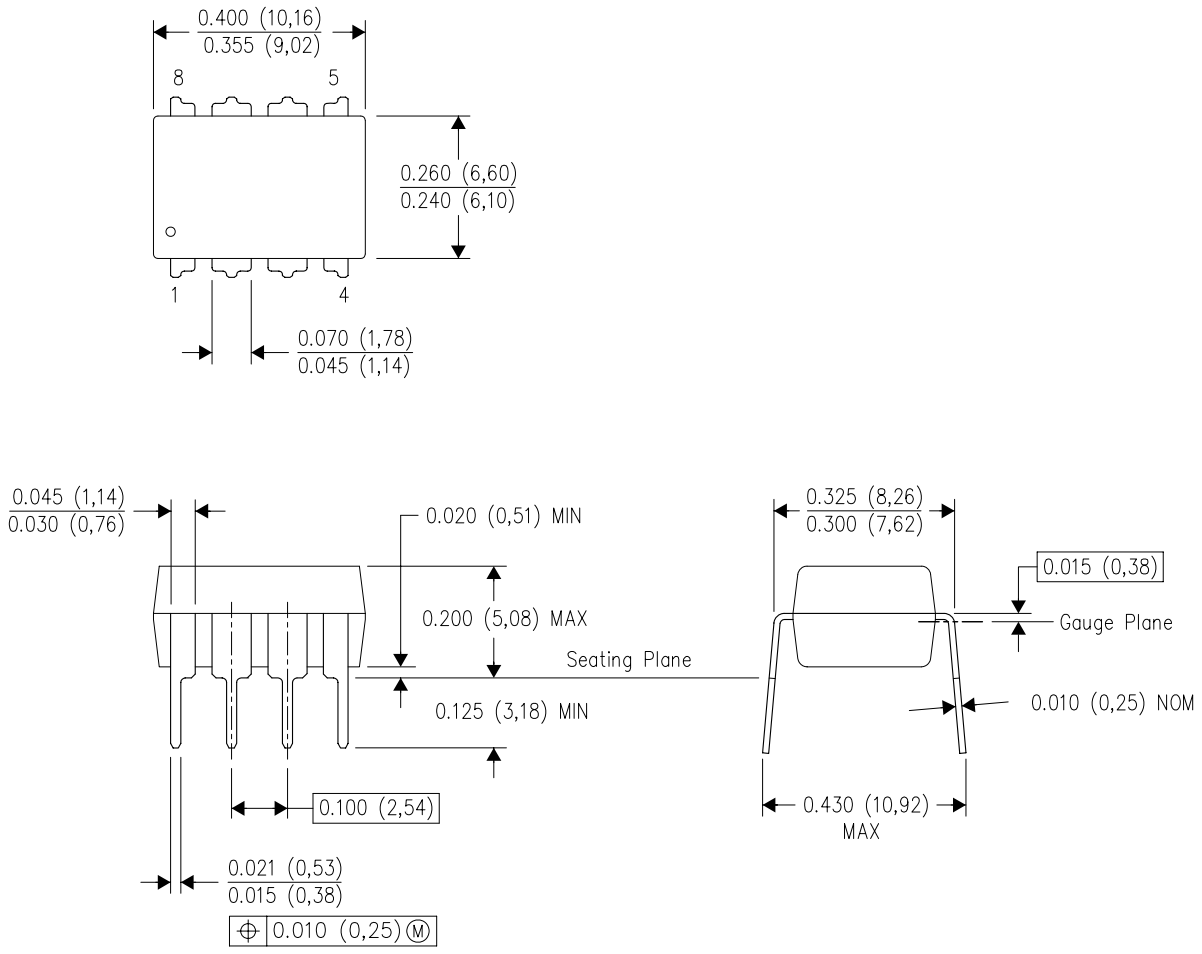
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)

FEATURES

- Slew Rate: 30V/µs
- Gain-Bandwidth Product: 35MHz
- Settling Time (0.01%): 3µs
- Overdrive Recovery: 0.4µs
- Gain Error: 0.05% Max
- Gain Drift: 5ppm/°C
- Gain Nonlinearity: 16ppm Max
- Offset Voltage (Input + Output): 600µV Max
  – Drift with Temperature: 2µV/°C
- Input Bias Current: 40pA Max
- Input Offset Current: 40pA Max
  – Drift with Temperature (to 70°C): 0.5pA/°C

APPLICATIONS

- Fast Settling Analog Signal Processing
- Multiplexed Input Data Acquisition Systems
- High Source Impedance Signal Amplification from High Resistance Bridges, Capacitance Sensors, Photodetector Sensors
- Bridge Amplifier with < 1Hz Lowpass Filtering

DESCRIPTION

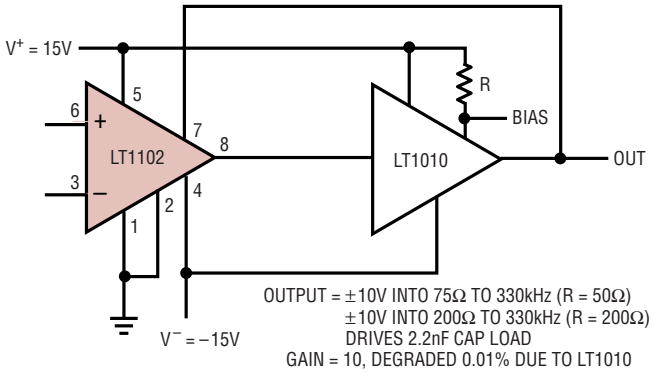
The LT®1102 is the first fast FET input instrumentation amplifier offered in the low cost, space saving 8-pin packages. Fixed gains of 10 and 100 are provided with excellent gain accuracy (0.01%) and non-linearity (3ppm). No external gain setting resistor is required.

Slew rate, settling time, gain-bandwidth product, overdrive recovery time are all improved compared to competitive high speed instrumentation amplifiers.

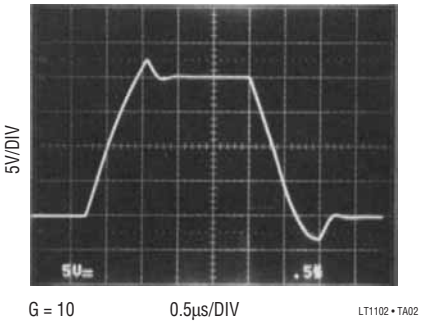
Industry best speed performance is combined with impressive precision specifications: less than 10pA input bias and offset currents, 180µV offset voltage. Unlike other FET input instrumentation amplifiers, on the LT1102 there is no output offset voltage contribution to total error, and input bias currents do not double with every 10°C rise in temperature. Indeed, at 70°C ambient temperature the input bias current is only 40pA.

TYPICAL APPLICATION

Wideband Instrumentation Amplifier with ±150mA Output Current



Slew Rate



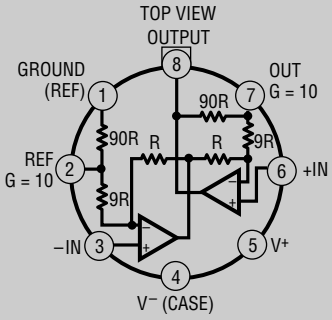
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
LT1102I ..... –40°C to 85°C
LT1102AC/LT1102C ..... 0°C to 70°C
LT1102AM/LT1102M **(OBSOLETE)**.....–55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

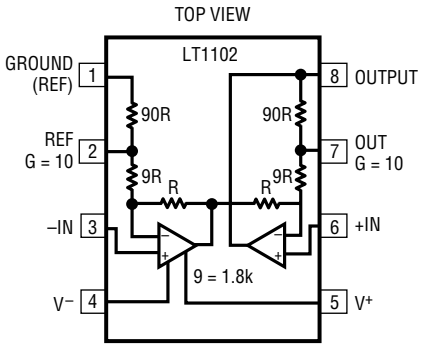


H PACKAGE
8-LEAD TO-5 METAL CAN

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

ORDER PART NUMBER

LT1102AMH
LT1102MH
LT1102ACH
LT1102CH



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1102IN8
LT1102ACN8
LT1102CN8

J8 PACKAGE
8-LEAD CERDIP

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

LT1102MJ8
LT1102CJ8

LT1102 • POI01

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, Gain = 10 or 100, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM/AC MIN	LT1102AM/AC TYP	LT1102AM/AC MAX	LT1102M/I/C MIN	LT1102M/I/C TYP	LT1102M/I/C MAX	UNITS
G_E	Gain Error	V_O = ±10V, R_L = 50k or 2k		0.010	0.050		0.012	0.070	%
G_{NL}	Gain Nonlinearity	G = 100, R_L = 50k G = 100, R_L = 2k G = 10, RL = 50k or 2k		3 8 7	14 20 16		4 8 7	18 25 30	ppm ppm ppm
V_{OS}	Input Offset Voltage			180	600		200	900	µV
I_{OS}	Input Offset Current			3	40		4	60	pA
I_B	Input Bias Current			±3	±40		±4	±60	pA
	Input Resistance Common Mode Differential Mode	 V_{CM} = –11V to 8V V_{CM} = 8V to 11V		 10^{12} 10^{11} 10^{12}			 10^{12} 10^{11} 10^{12}		 Ω Ω Ω
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.8			2.8		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz (Note 2)		37 19	 30		37 20		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Input Noise Current Density	f_O = 1000Hz, 10Hz (Note 3)		1.5	4		2	5	$fA/\sqrt{Hz}$
	Input Voltage Range		±10.5	±11.5		±10.5	±11.5		V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = ±10.5V	84	98		82	97		dB
PSRR	Power Supply Rejection Ratio	V_S = ±9V to ±18V	88	102		86	101		dB
I_S	Supply Current			3.3	5.0		3.4	5.6	mA
V_O	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±13.0 ±12.0	±13.5 ±13.0		±13.0 ±12.0	±13.5 ±13.0		V V
BW	Bandwidth	G = 100 (Note 4) G = 10 (Note 4)	120 2.0	220 3.5		100 1.7	220 3.5		kHz MHz
SR	Slew Rate	G = 100, V_{IN} = ±0.13V, V_O = ±5V G = 10, V_{IN} = ±1V, V_O = ±5V	12 21	17 30		10 18	17 30		V/µs V/µs
	Overdrive Recovery	50% Overdrive (Note 5)		400			400		ns
	Settling Time	V_O = 20V Step (Note 4) G = 10 to 0.05% G = 10 to 0.01% G = 100 to 0.05% G = 100 to 0.01%		 1.8 3.0 7 9	 4.0 6.5 13 18		 1.8 3.0 7 9	 4.0 6.5 13 18	 µs µs µs µs

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $-55°C \le T_A \le 125°C$ for AM/M grades, $-40°C \le T_A \le 85°C$ for I grades, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM MIN	LT1102AM TYP	LT1102AM MAX	LT1102M/I MIN	LT1102M/I TYP	LT1102M/I MAX	UNITS
G_E	Gain Error	G = 100, $V_O = \pm 10V$, R_L = 50k or 2k G = 10, $V_O = \pm 10V$, R_L = 50k or 2k		0.10 0.05	0.25 0.12		0.10 0.06	0.30 0.15	% %
TCG_E	Gain Error Drift (Note 6)	G = 100, R_L = 50k or 2k G = 10, R_L = 50k or 2k		9 5	20 10		10 6	25 14	ppm/°C ppm/°C
G_{NL}	Gain Nonlinearity	G = 100, R_L = 50k G = 100, R_L = 2k G = 10, R_L = 50k or 2k		20 28 9	70 85 20		24 32 9	90 110 24	ppm ppm ppm
V_{OS}	Input Offset Voltage			300	1400		400	2000	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	µV/°C
I_{OS}	Input Offset Current			0.3	4		0.4	6	nA
I_B	Input Bias Current			±2	±10		±2.5	±15	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	82	97		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	88	100		84	99		dB
I_S	Supply Current	$T_A = 125°C$		2.5			2.5		mA
V_O	Maximal Output Voltage Swing	R_L = 50k R_L = 2k	±12.5 ±12.0	±13.2 ±12.6		±12.5 ±12.0	±13.2 ±12.6		V V

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AC MIN	LT1102AC TYP	LT1102AC MAX	LT1102C MIN	LT1102C TYP	LT1102C MAX	UNITS
G_E	Gain Error	G = 100, $V_O = \pm 10V$, R_L = 50k or 2k G = 10, $V_O = \pm 10V$, R_L = 50k or 2k		0.04 0.03	0.11 0.09		0.05 0.04	0.14 0.12	% %
TCG_E	Gain Error Drift (Note 6)	G = 100, R_L = 50k or 2k G = 10, R_L = 50k or 2k		8 5	18 10		9 6	22 14	ppm/°C ppm/°C
G_{NL}	Gain Nonlinearity	G = 100, R_L= 50k G = 100, R_L= 2k G = 10, R_L= 50k or 2k		8 11 8	30 36 18		9 12 8	40 48 22	ppm ppm ppm
V_{OS}	Input Offset Voltage			230	1000		280	1400	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	µV/°C
I_{OS}	Input Offset Current			10	150		15	220	pA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 6)		0.5	3		0.5	4	pA/°C
I_B	Input Bias Current			±40	±300		±50	±400	pA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 6)		1	4		1	6	pA/°C
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	83	98		81	97		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	87	101		85	100		dB
I_S	Supply Current	$T_A = 70°C$		2.8			2.9		mA
V_O	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±12.8 ±12.0	±13.4 ±12.8		±12.8 ±12.0	±13.4 ±12.8		V V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula:

$i_n = (2qI_B)^{1/2}$

where $q = 1.6 \bullet 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 4: This parameter is not tested. It is guaranteed by design and by inference from the slew rate measurement.

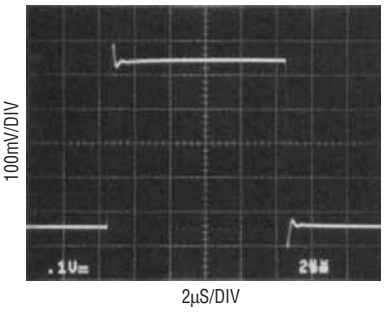
Note 5: Overdrive recovery is defined as the time delay from the removal of an input overdrive to the output's return from saturation to linear operation.

50% overdrive equals $V_{IN} = \pm 2V$ (G = 10) or $V_{IN} = \pm 200mV$ (G = 100).

Note 6: This parameter is not tested. It is guaranteed by design and by inference from other tests.

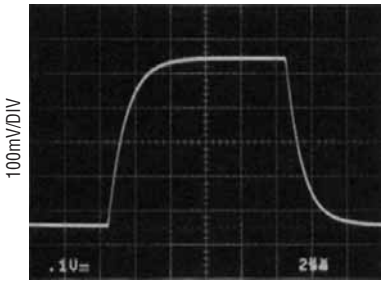
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Response, G = 10 (Input = 50mV Pulse)



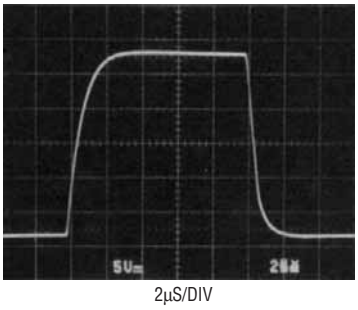
LT1102 • TPC01

Small Signal Response, G = 100 (Input = 5mV Pulse)



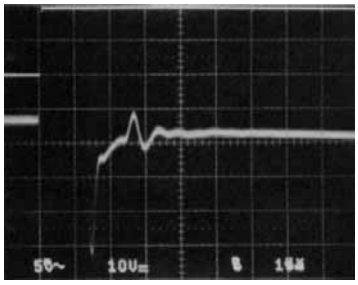
LT1102 • TPC02

Slew Rate, G = 100 (Input = ±130mV Pulse)



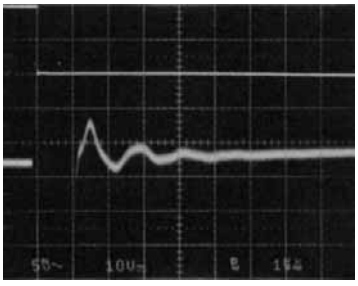
LT1102 • TPC03

Settling Time, G = 10 (Input From –10V to 10V)



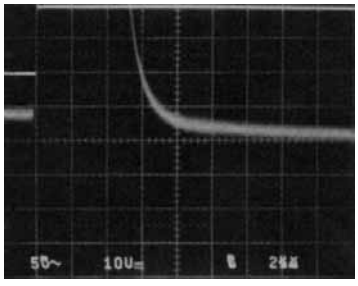
LT1102 • TPC04

Settling Time, G = 10 (Input From 10V to –10V)



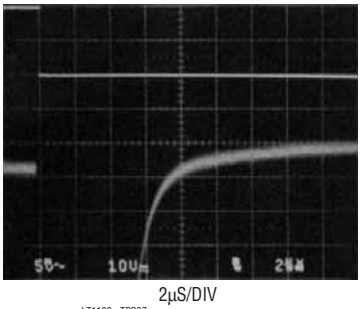
LT1102 • TPC05

Settling Time, G = 100 (Input From –10V to 10V)



LT1102 • TPC06

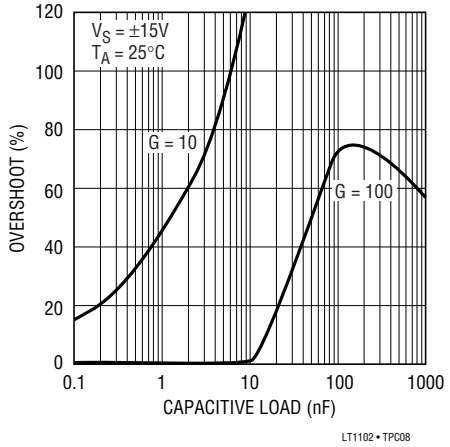
Settling Time, G = 100 (Input From 10V to –10V)



LT1102 • TPC07

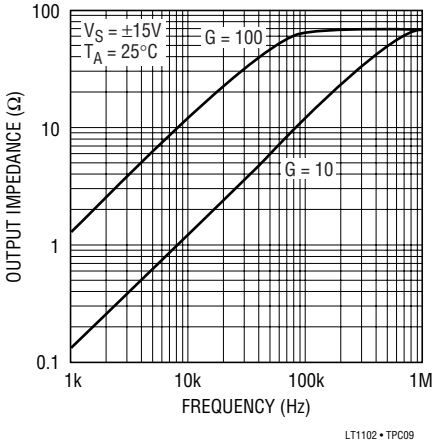
TYPICAL PERFORMANCE CHARACTERISTICS

Capacitive Load Handling



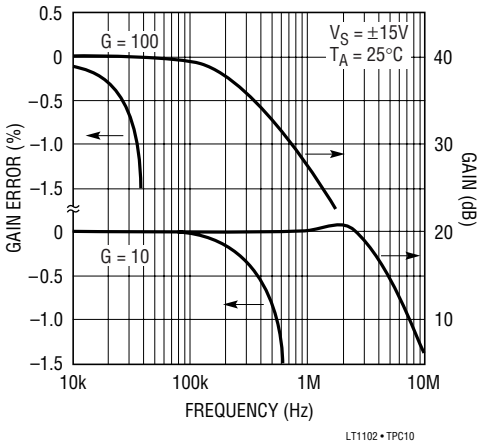
LT1102 • TPC08

Output Impedance vs Frequency



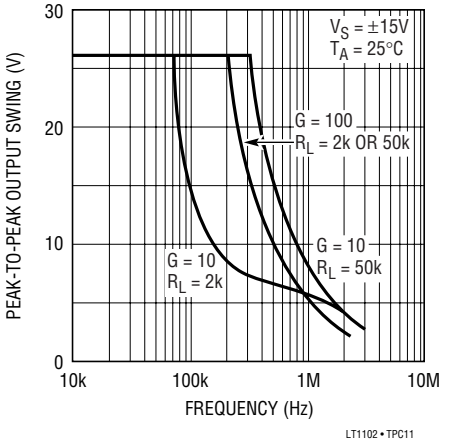
LT1102 • TPC09

Gain vs Frequency



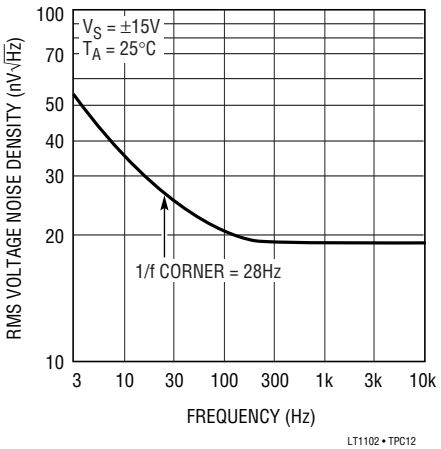
LT1102 • TPC10

Undistorted Output vs Frequency



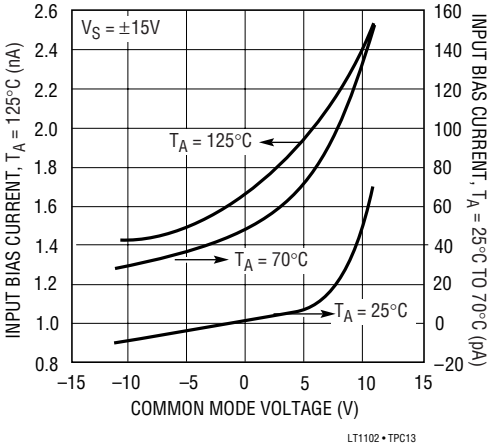
LT1102 • TPC11

Voltage Noise vs Frequency



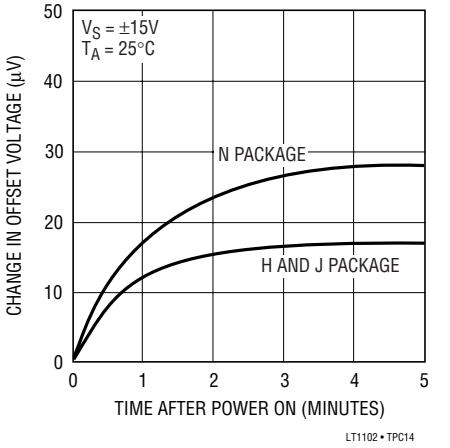
LT1102 • TPC12

Input Bias Current Over the Common Mode Range



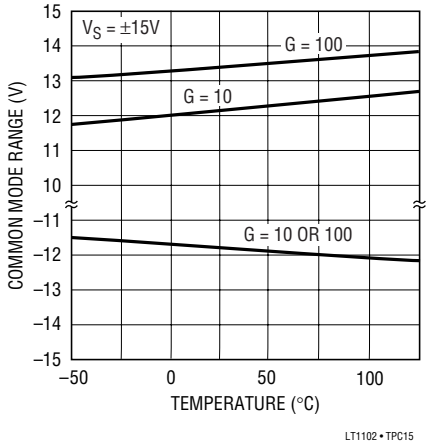
LT1102 • TPC13

Warm-Up Drift



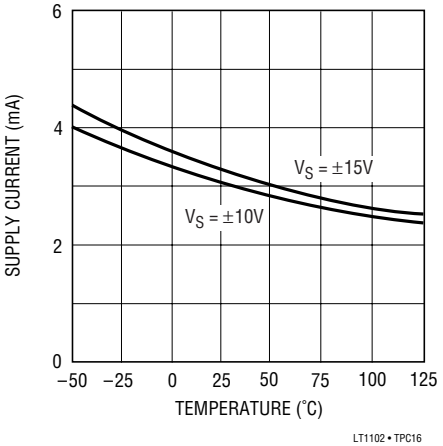
LT1102 • TPC14

Common Mode Range vs Temperature



LT1102 • TPC15

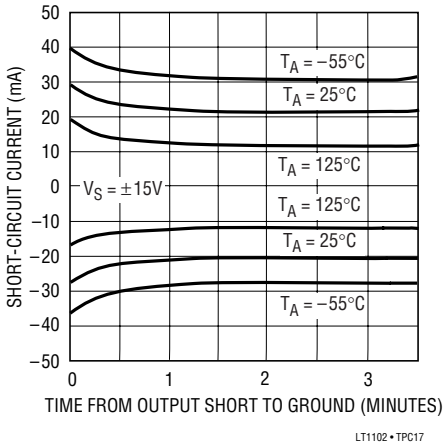
Supply Current vs Temperature



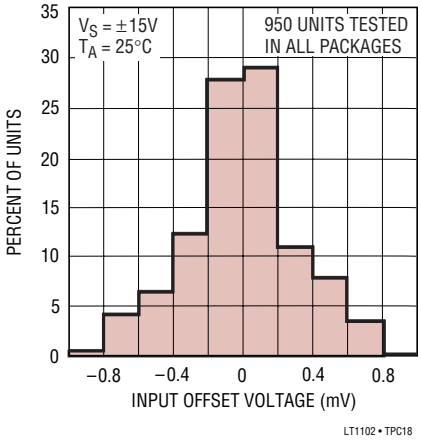
LT1102 • TPC16

TYPICAL PERFORMANCE CHARACTERISTICS

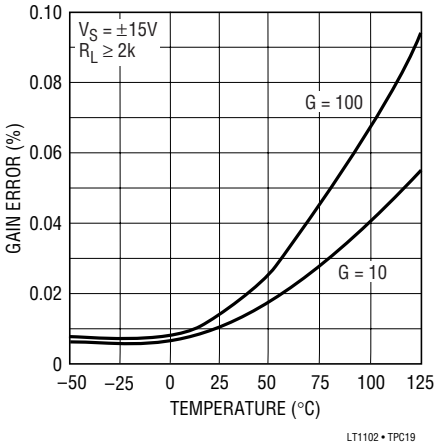
Short-Circuit Current vs Time



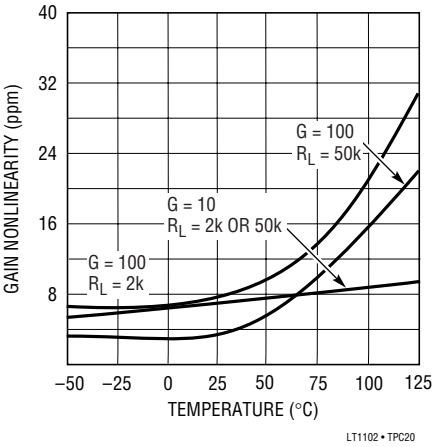
Distribution of Offset Voltage



Gain Error vs Temperature



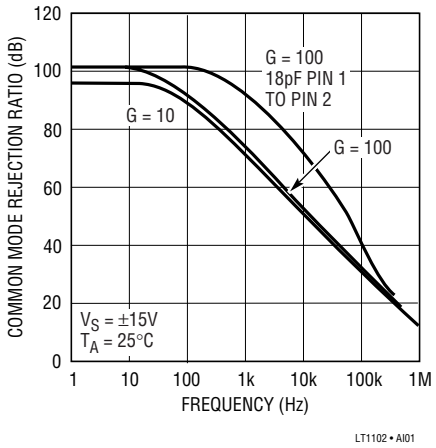
Gain Nonlinearity Over Temperature



APPLICATIONS INFORMATION

In the two op amp instrumentation amplifier configuration, the first amplifier is basically in unity gain, and the second amplifier provides all the voltage gain. In the LT1102, the second amplifier is decompensated for gain of 10 stability, therefore high slew rate and bandwidth are achieved. Common mode rejection versus frequency is also optimized in the G = 10 mode, because the bandwidths of the two op amps are similar. When G = 100, this statement is no longer true; however, by connecting an 18pF capacitor between pins 1 and 2, a common mode AC gain is created to cancel the inherent roll-off. From 200Hz to 30kHz, CMRR versus frequency is improved by an order of magnitude.

Common Mode Rejection Ratio vs Frequency



Input Protection

Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1102 employs FET input transistors, consequently the differential input voltage can be ±30V (with ±15V supplies, ±36V with ±18V supplies). Some competitive instrumentation amplifiers have NPN inputs which are protected by back-to-back diodes. When the differential input Voltage exceeds ±13V on these competitive devices, input current increases to milliampere level; more than ±10V differential voltage can cause permanent damage.

When the LT1102 inputs are pulled below the negative supply or above the positive supply, the inputs will clamp a diode voltage below or above the supplies. No damage will occur if the input current is limited to 20mA.

Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors (= R_X) between pins 1 and 2 and pins 7 and 8.

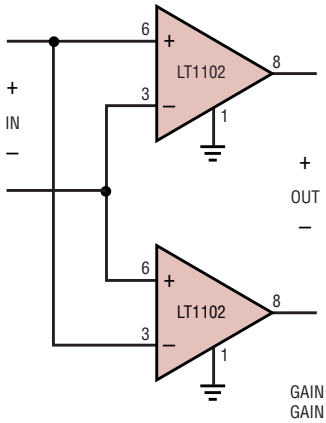
$$\text{Gain} = 10 + \frac{R_X}{R + R_X/90}$$

The nominal value of R is 1.84kΩ. The usefulness of this method is limited by the fact that R is not controlled to better than ±10% absolute accuracy in production. However, on any specific unit, 90R can be measured between Pins 1 and 2.

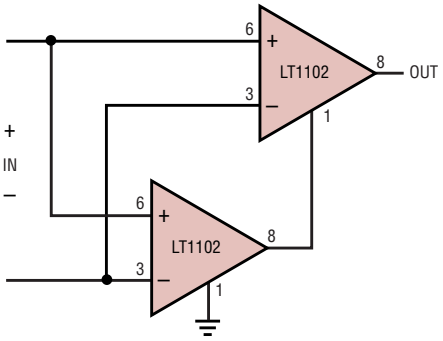
APPLICATIONS INFORMATION

Gain = 20, 110, or 200 Instrumentation Amplifiers

Differential Output



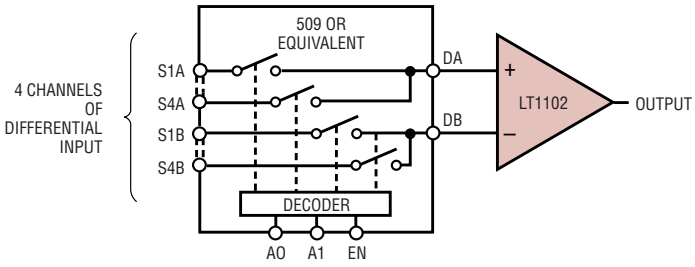
Single Ended Output



GAIN = 200, AS SHOWN
GAIN = 20, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON BOTH DEVICES
GAIN = 110, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON ONE DEVICE, NOT ON THE OTHER
INPUT REFERRED NOISE IS REDUCED BY √2 (G = 200 OR 20)

LT1102 • AI02

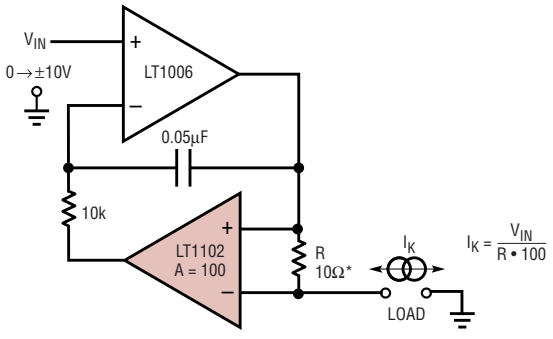
Multiplexed Input Data Acquisition



800kHz SIGNALS CAN BE MULTIPLEXED WITH LT1102 IN G = 10

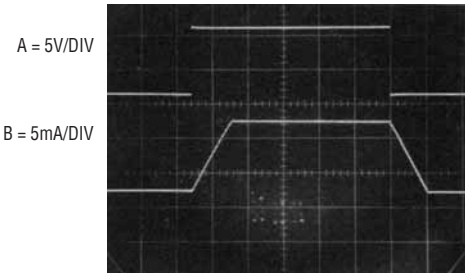
LT1102 • AI03

Voltage Programmable Current Source is Simple and Precise



LT1102 • AI04

Dynamic Response of the Current Source

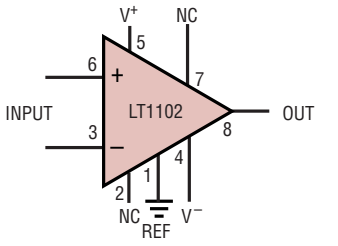


HORIZ. = 20µs/DIV

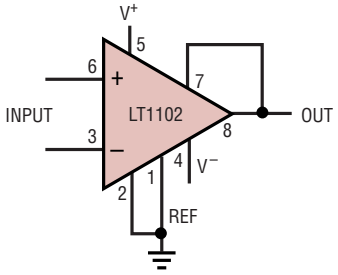
LT1102 • AI05

TYPICAL APPLICATIONS

Basic Connections



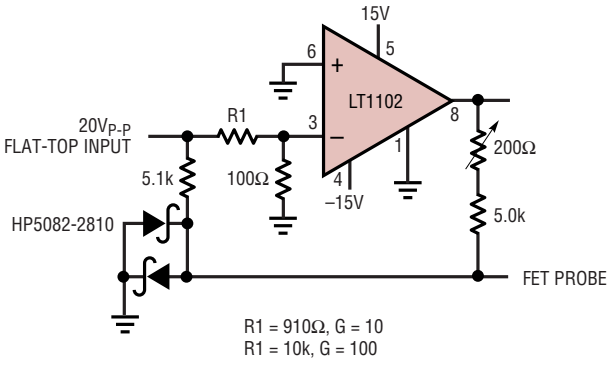
GAIN = 100



GAIN = 10

LT1102 • TA03

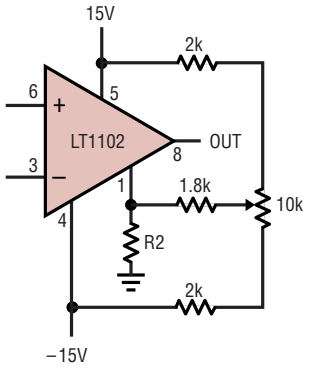
Settling Time Test Circuit



R1 = 910Ω, G = 10
R1 = 10k, G = 100

LT1102 • TA04

Offset Nulling

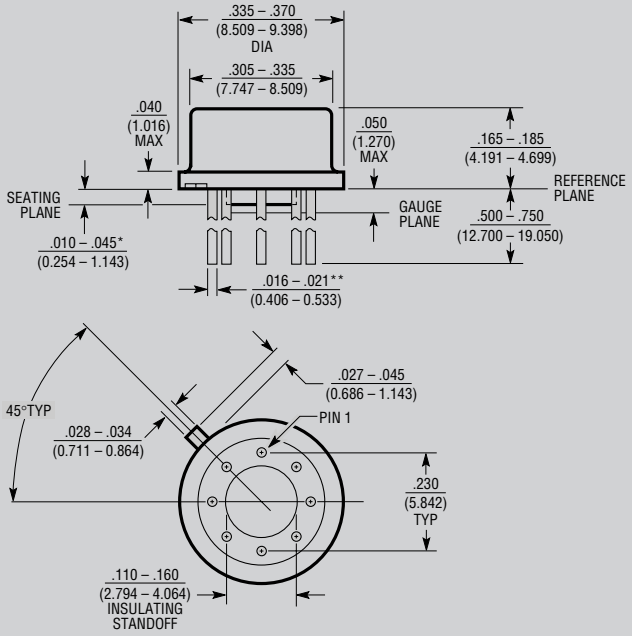


R2 = 3.3Ω, G = 10
R2 = 30Ω, G = 100
NULL RANGE = ±1mV
GAIN DEGRADATION ≈ 0.018%

LT1102 • TA05

PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.230 Inch PCD)
(Reference LTC DWG # 05-08-1321)

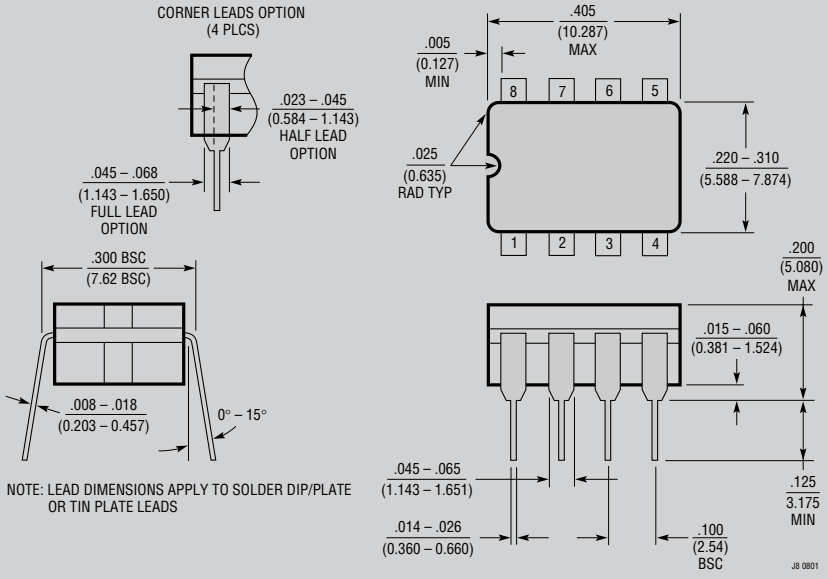


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS .016 – .024 (0.406 – 0.610)

H8 (TO-5) 0.230 PCD 0801

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

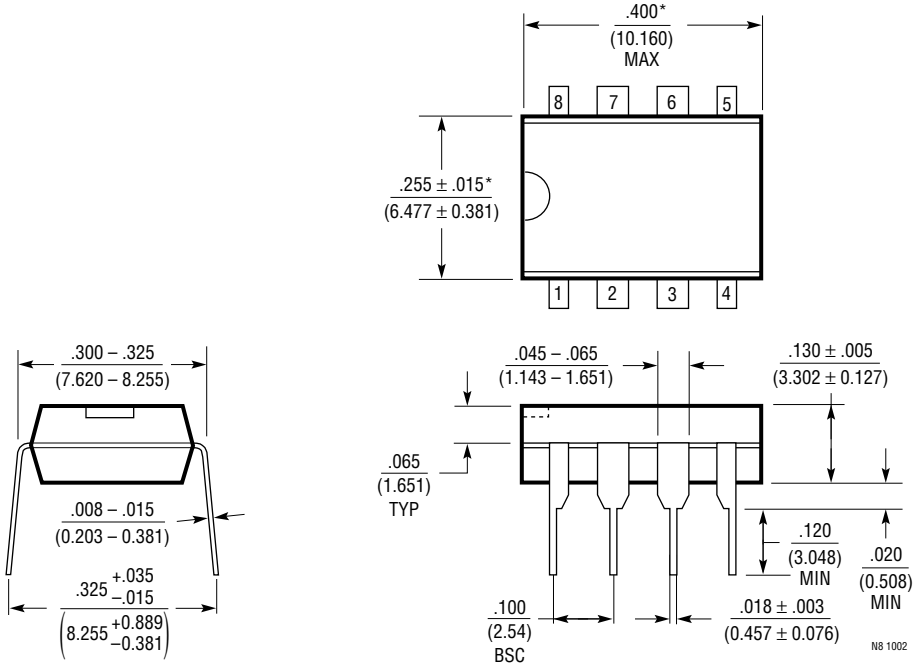


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

OBSOLETE PACKAGES

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

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LT 0507 REV B • PRINTED IN USA

SPECIFICATIONS

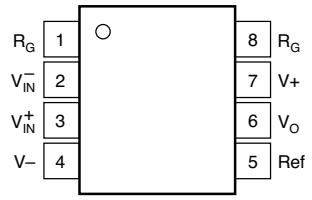
At T_A = +25°C, V_S = +5V, R_L = 20kΩ connected to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	INA122P, U			INA122PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI			±100	±250		±150	±500	µV
vs Temperature			±1	±3		*	±5	µV/°C
vs Power Supply (PSRR)	V_S = +2.2V to +36V		10	30		*	100	µV/V
Input Impedance			10^{10} ll 3			*		Ω ll pF
Safe Input Voltage	R_S = 0	(V–)–0.3		(V+)+0.3	*		*	V
	R_S = 10kΩ	(V–)–40		(V+)+40	*		*	V
Common-Mode Voltage Range		0		3.4	*		*	V
Common-Mode Rejection	V_{CM} = 0V to 3.4V	83	96		76	90		dB
INPUT BIAS CURRENT			–10	–25		*	–50	nA
vs Temperature			±40			*		pA/°C
Offset Current			±1	±2		*	±5	nA
vs Temperature			±40			*		pA/°C
GAIN			G = 5 to 10k			*		V/V
Gain Equation			G = 5 + 200kΩ/R_G			*		V/V
Gain Error	G = 5		±0.05	±0.1		*	±0.15	%
vs Temperature	G = 5		5	10		*	*	ppm/°C
Gain Error	G = 100		±0.3	±0.5		*	±1	%
vs Temperature	G = 100		±25	±100		*	*	ppm/°C
Nonlinearity	G = 100, V_O = –14.85V to +14.9V		±0.005	±0.012		*	±0.024	%
NOISE (RTI)								
Voltage Noise, f = 1kHz			60			*		nV/√Hz
f = 100Hz			100			*		nV/√Hz
f = 10Hz			110			*		nV/√Hz
f_B = 0.1Hz to 10Hz			2			*		µVp-p
Current Noise, f = 1kHz			80			*		fA/√Hz
f_B = 0.1Hz to 10Hz			2			*		pAp-p
OUTPUT								
Voltage, Positive	V_S = ±15V	(V+)–0.1	(V+)–0.05		*	*		V
Negative	V_S = ±15V	(V–)+0.15	(V–)+0.1		*	*		V
Short-Circuit Current	Short-Circuit to Ground		+3/–30			*		mA
Capacitive Load Drive			1			*		nF
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 5		120			*		kHz
	G = 100		5			*		kHz
	G = 500		0.9			*		kHz
Slew Rate			+0.08/–0.16			*		V/µs
Settling Time, 0.01%	G = 5		350			*		µs
	G = 100		450			*		µs
	G = 500		1.8			*		ms
Overload Recovery	50% Input Overload		3			*		µs
POWER SUPPLY								
Voltage Range, Single Supply		+2.2	+5	+36	*	*	*	V
Dual Supplies		–0.9/+1.3		±18	*	*	*	V
Current	I_O = 0		60	85		*	*	µA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operation		–55		+85	*		*	°C
Storage		–55		+125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Pin DIP			150			*		°C/W
SO-8 Surface-Mount			150			*		°C/W

* Specification same as INA122P, INA122U.

PIN CONFIGURATION

Top View **8-Pin DIP, SO-8**



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Signal Input Terminals, Voltage[2]	(V–)–0.3V to (V+)+0.3V
Current[2]	5mA
Output Short Circuit	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are internally diode-clamped to the power supply rails. Input signals that can exceed the supply rails by more than 0.3V should be current-limited to 5mA or less.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
INA122PA	8-Pin DIP	006
INA122P	8-Pin DIP	006
INA122UA	SO-8 Surface Mount	182
INA122U	SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

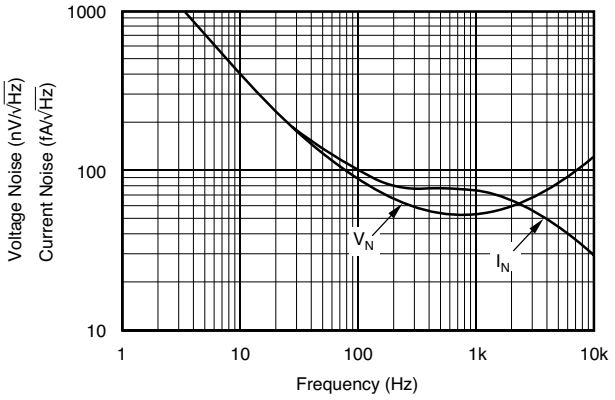
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

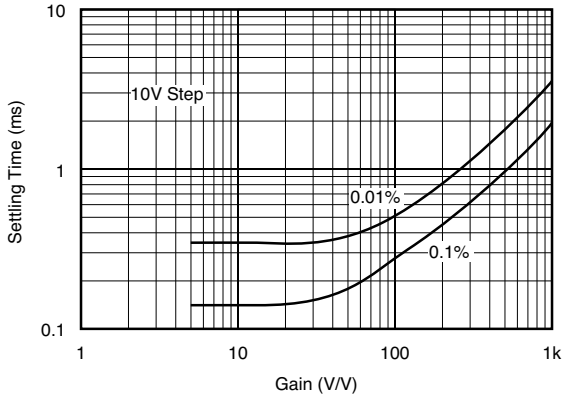
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C and V_S = ±5V, unless otherwise noted.

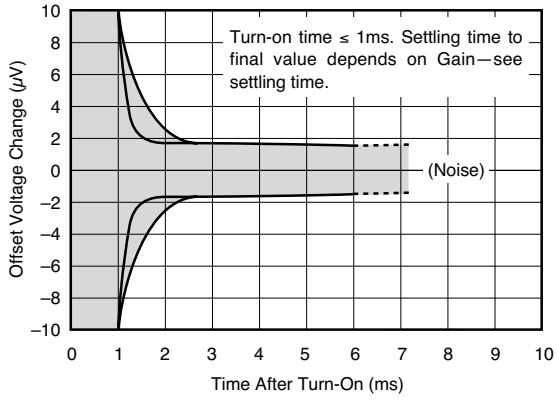
VOLTAGE and CURRENT NOISE DENSITY vs FREQUENCY (RTI)



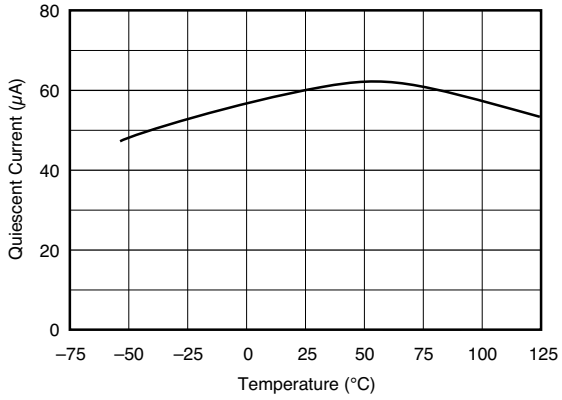
SETTLING TIME vs GAIN



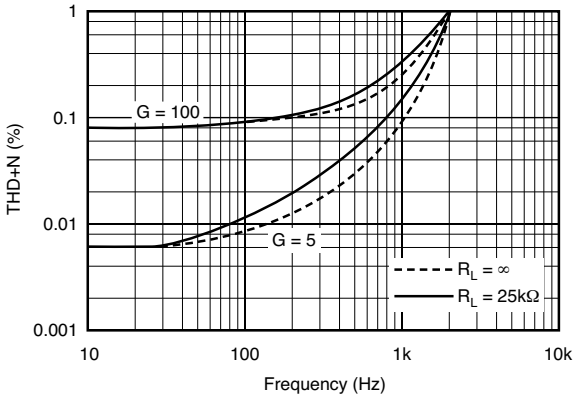
INPUT-REFERRED OFFSET VOLTAGE WARM-UP



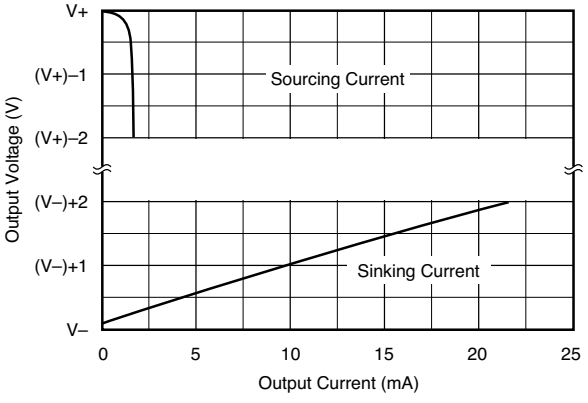
QUIESCENT CURRENT vs TEMPERATURE



TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

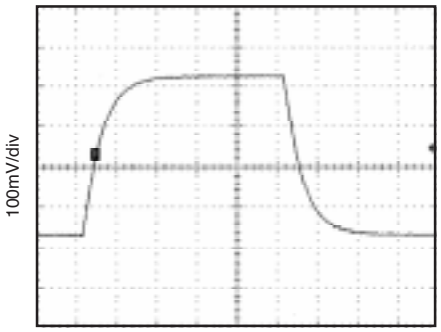


TYPICAL PERFORMANCE CURVES (CONT)

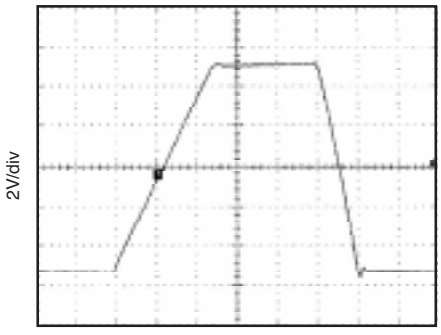
At T_A = +25°C and V_S = ±5V, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE
G = 5

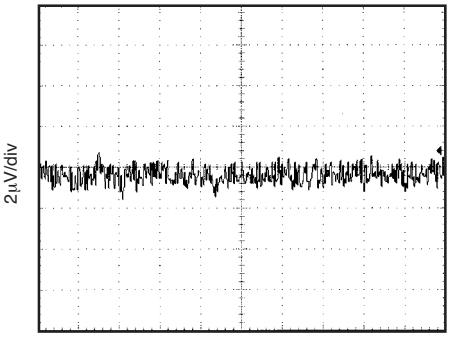
SMALL-SIGNAL STEP RESPONSE
G = 100



LARGE-SIGNAL STEP RESPONSE
G = 5



INPUT-REFERRED NOISE VOLTAGE
0.1Hz to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA122. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to ensure good common-mode rejection. A resistance of 10Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR.

SETTING THE GAIN

Gain of the INA122 is set by connecting a single external resistor, R_G, as shown:

$$G = 5 + \frac{200k\Omega}{R_G} \quad (1)$$

Commonly used gains and R_G resistor values are shown in Figure 1.

The 200kΩ term in equation 1 comes from the internal metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA122.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1).

OFFSET TRIMMING

The INA122 is laser trimmed for low offset voltage and offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.

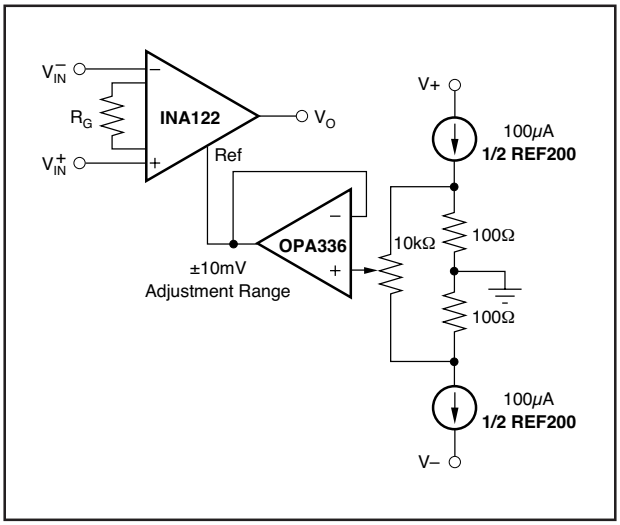


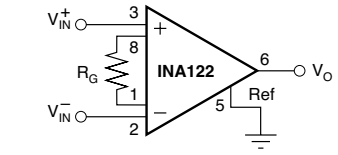
FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA122 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately –10nA (current flows out of the input terminals). High input impedance means that this input bias current changes very little with varying input voltage.

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G VALUE
5	NC	NC
10	40k	40.2k
20	13.33k	13.3k
50	4444	4420
100	2105	2100
200	1026	1020
500	404	402
1000	201	200
2000	100.3	100
5000	40	40.2
10000	20	20

NC: No Connection.



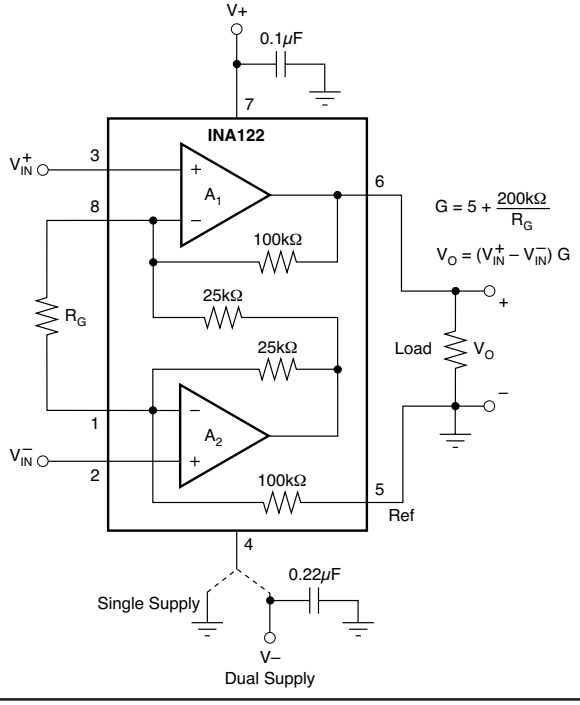


FIGURE 1. Basic Connections.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA122 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

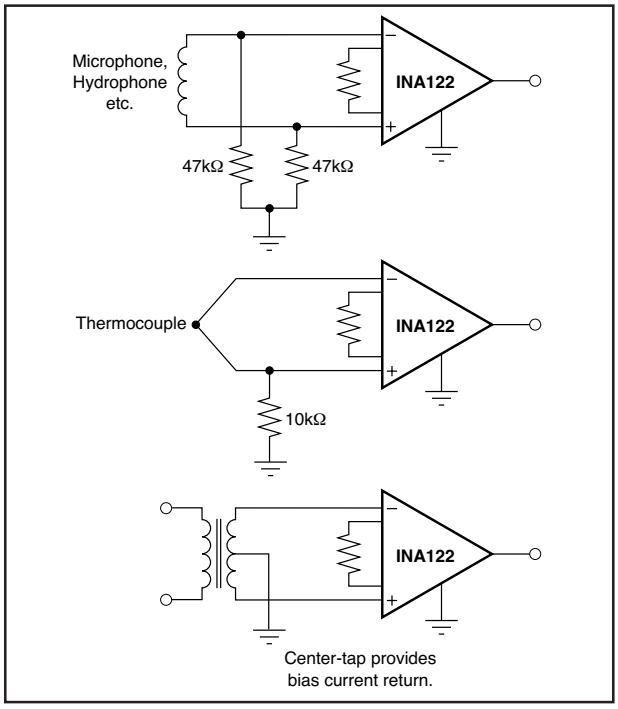


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT PROTECTION

The inputs of the INA122 are protected with internal diodes connected to the power supply rails (Figure 4). These diodes will clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.3V, the input signal current should be limited to less than 5mA to protect the internal clamp diodes. This can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

INPUT COMMON-MODE RANGE

The common-mode range for some common operating conditions is shown in the typical performance curves. The INA122 can operate over a wide range of power supply and V_{REF} configurations, making it impractical to provide a comprehensive guide to common-mode range limits for all possible conditions. The most commonly overlooked overload condition occurs by attempting to exceed the output swing of A_2, an internal circuit node that cannot be measured. Calculating the expected voltages at A_2's output (see equation in Figure 4) provides a check for the most common overload conditions.

The design of A_1 and A_2 are identical and their outputs can swing to within approximately 100mV of the power supply rails, depending on load conditions. When A_2's output is saturated, A_1 can still be in linear operation, responding to changes in the non-inverting input voltage. This may give the appearance of linear operation but the output voltage is invalid.

A single supply instrumentation amplifier has special design considerations. Using commonly available single-supply op amps to implement the two-op amp topology will not yield equivalent performance. For example, consider the condition where both inputs of common single-supply op amps are

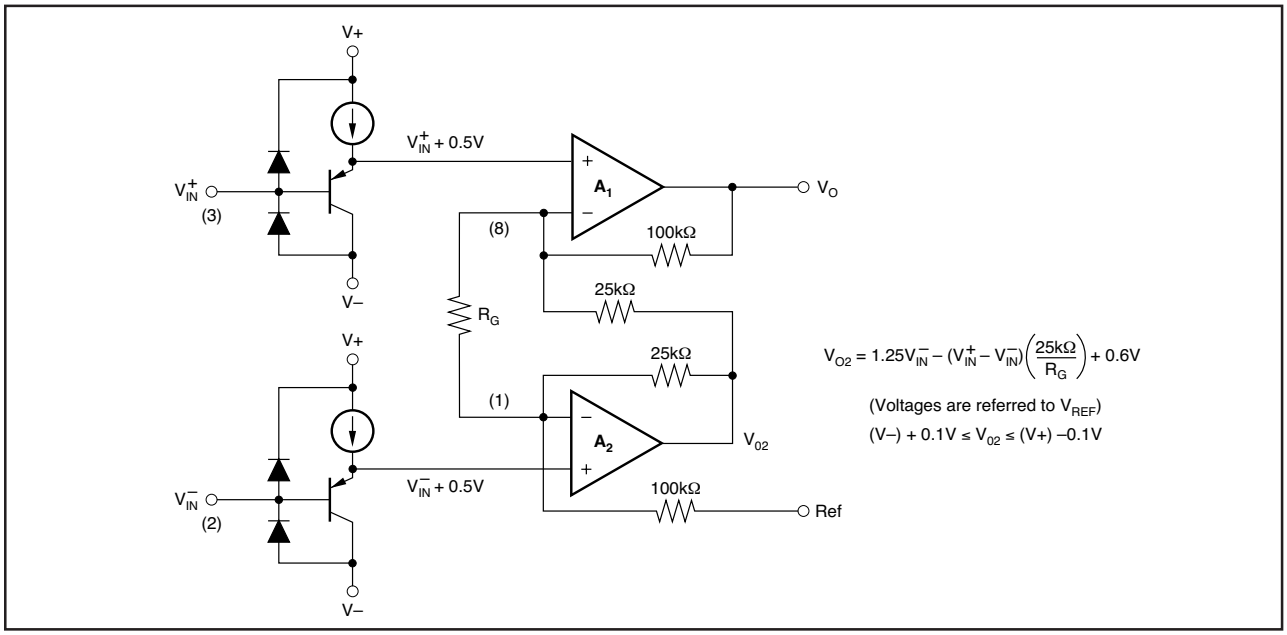


FIGURE 4. INA122 Simplified Circuit Diagram.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA122P	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	INA122P	
INA122PA	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA122P A	
INA122PAG4	LIFEBUY	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA122P A	
INA122U	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U	
INA122U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U	Samples
INA122UA	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U A	
INA122UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-3-260C-168 HR		INA 122U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

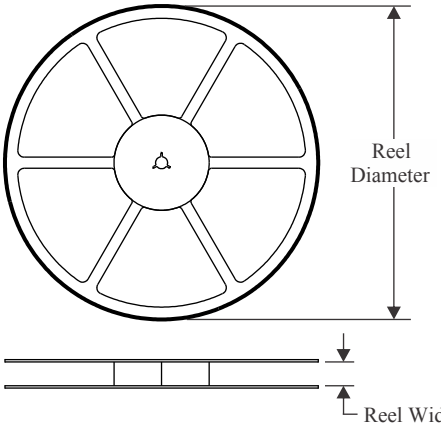
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

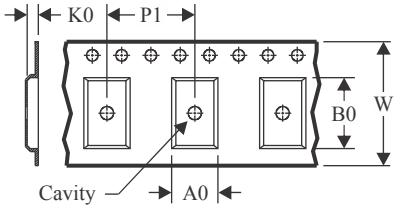
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

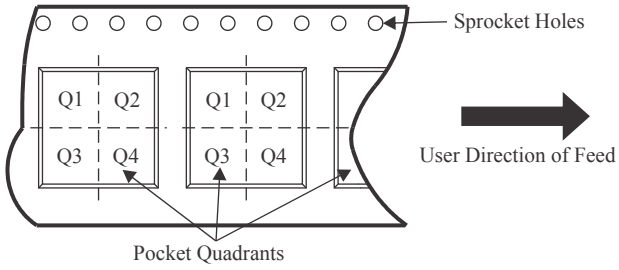


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

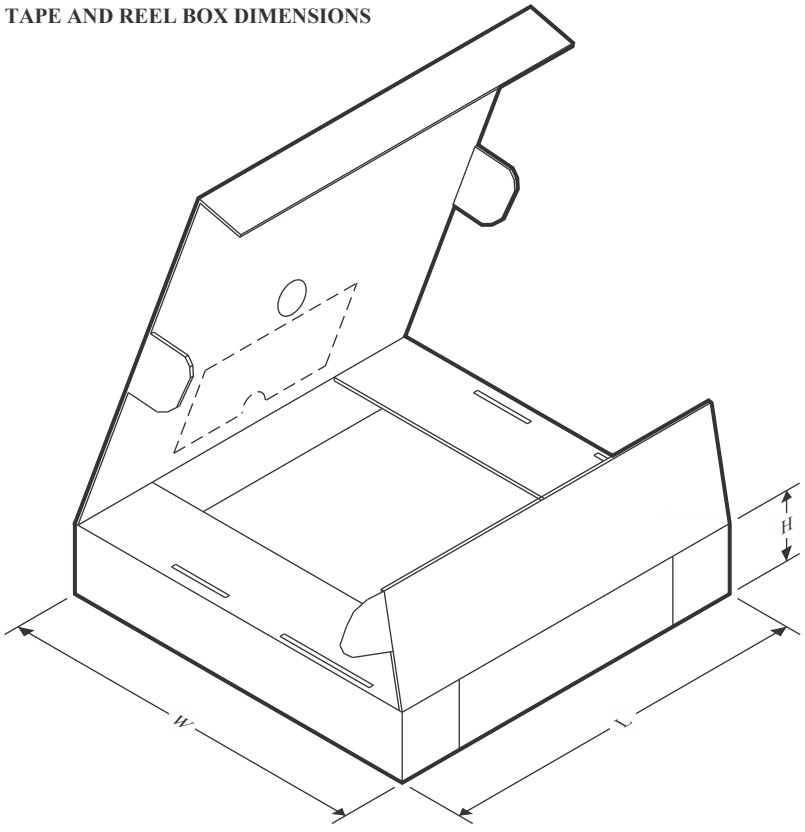
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA122U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA122UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

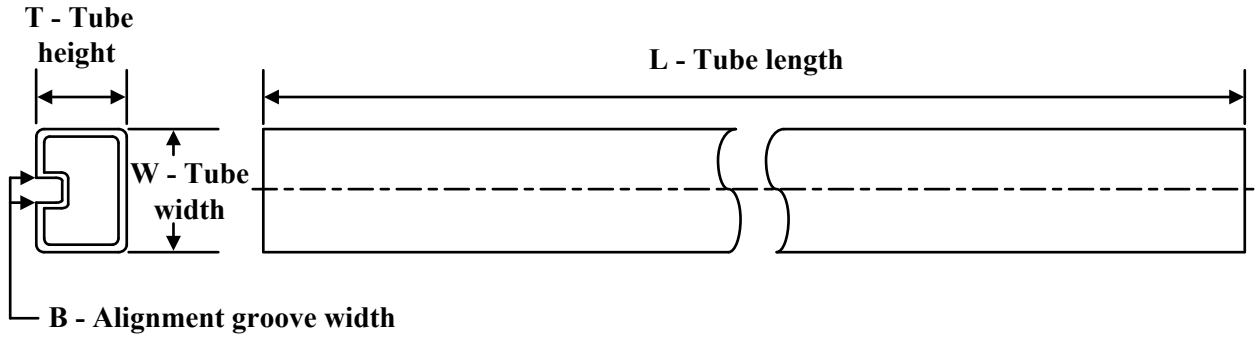
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA122U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA122UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA122P	P	PDIP	8	50	506	13.97	11230	4.32
INA122PA	P	PDIP	8	50	506	13.97	11230	4.32
INA122PAG4	P	PDIP	8	50	506	13.97	11230	4.32
INA122U	D	SOIC	8	75	506.6	8	3940	4.32
INA122UA	D	SOIC	8	75	506.6	8	3940	4.32

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)

FEATURES

- Slew Rate: 30V/µs
- Gain-Bandwidth Product: 35MHz
- Settling Time (0.01%): 3µs
- Overdrive Recovery: 0.4µs
- Gain Error: 0.05% Max
- Gain Drift: 5ppm/°C
- Gain Nonlinearity: 16ppm Max
- Offset Voltage (Input + Output): 600µV Max
  – Drift with Temperature: 2µV/°C
- Input Bias Current: 40pA Max
- Input Offset Current: 40pA Max
  – Drift with Temperature (to 70°C): 0.5pA/°C

APPLICATIONS

- Fast Settling Analog Signal Processing
- Multiplexed Input Data Acquisition Systems
- High Source Impedance Signal Amplification from High Resistance Bridges, Capacitance Sensors, Photodetector Sensors
- Bridge Amplifier with < 1Hz Lowpass Filtering

DESCRIPTION

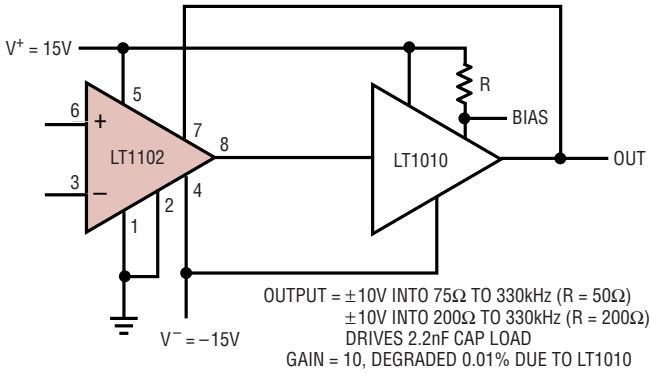
The LT®1102 is the first fast FET input instrumentation amplifier offered in the low cost, space saving 8-pin packages. Fixed gains of 10 and 100 are provided with excellent gain accuracy (0.01%) and non-linearity (3ppm). No external gain setting resistor is required.

Slew rate, settling time, gain-bandwidth product, overdrive recovery time are all improved compared to competitive high speed instrumentation amplifiers.

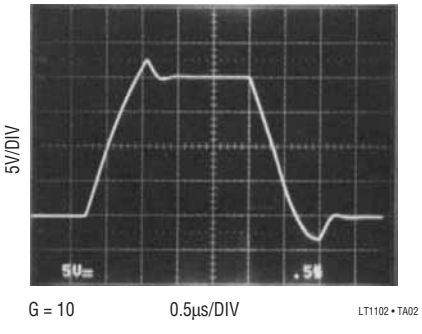
Industry best speed performance is combined with impressive precision specifications: less than 10pA input bias and offset currents, 180µV offset voltage. Unlike other FET input instrumentation amplifiers, on the LT1102 there is no output offset voltage contribution to total error, and input bias currents do not double with every 10°C rise in temperature. Indeed, at 70°C ambient temperature the input bias current is only 40pA.

TYPICAL APPLICATION

Wideband Instrumentation Amplifier with ±150mA Output Current



Slew Rate



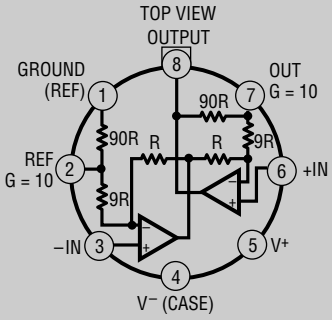
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
LT1102I ..... –40°C to 85°C
LT1102AC/LT1102C ..... 0°C to 70°C
LT1102AM/LT1102M **(OBSOLETE)**.....–55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

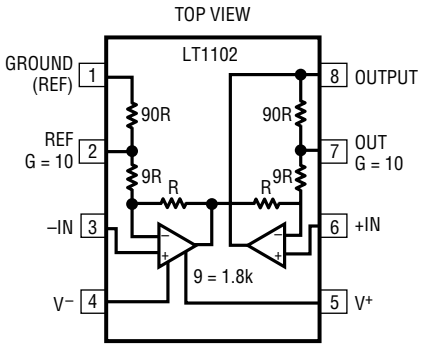


H PACKAGE
8-LEAD TO-5 METAL CAN

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

ORDER PART NUMBER

LT1102AMH
LT1102MH
LT1102ACH
LT1102CH



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1102IN8
LT1102ACN8
LT1102CN8

J8 PACKAGE
8-LEAD CERDIP

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

LT1102MJ8
LT1102CJ8

LT1102 • POI01

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, Gain = 10 or 100, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM/AC MIN	LT1102AM/AC TYP	LT1102AM/AC MAX	LT1102M/I/C MIN	LT1102M/I/C TYP	LT1102M/I/C MAX	UNITS
G_E	Gain Error	V_O = ±10V, R_L = 50k or 2k		0.010	0.050		0.012	0.070	%
G_{NL}	Gain Nonlinearity	G = 100, R_L = 50k G = 100, R_L = 2k G = 10, RL = 50k or 2k		3 8 7	14 20 16		4 8 7	18 25 30	ppm ppm ppm
V_{OS}	Input Offset Voltage			180	600		200	900	µV
I_{OS}	Input Offset Current			3	40		4	60	pA
I_B	Input Bias Current			±3	±40		±4	±60	pA
	Input Resistance Common Mode Differential Mode	 V_{CM} = –11V to 8V V_{CM} = 8V to 11V		 10^{12} 10^{11} 10^{12}			 10^{12} 10^{11} 10^{12}		 Ω Ω Ω
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.8			2.8		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz (Note 2)		37 19	 30		37 20		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Input Noise Current Density	f_O = 1000Hz, 10Hz (Note 3)		1.5	4		2	5	$fA/\sqrt{Hz}$
	Input Voltage Range		±10.5	±11.5		±10.5	±11.5		V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = ±10.5V	84	98		82	97		dB
PSRR	Power Supply Rejection Ratio	V_S = ±9V to ±18V	88	102		86	101		dB
I_S	Supply Current			3.3	5.0		3.4	5.6	mA
V_O	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±13.0 ±12.0	±13.5 ±13.0		±13.0 ±12.0	±13.5 ±13.0		V V
BW	Bandwidth	G = 100 (Note 4) G = 10 (Note 4)	120 2.0	220 3.5		100 1.7	220 3.5		kHz MHz
SR	Slew Rate	G = 100, V_{IN} = ±0.13V, V_O = ±5V G = 10, V_{IN} = ±1V, V_O = ±5V	12 21	17 30		10 18	17 30		V/µs V/µs
	Overdrive Recovery	50% Overdrive (Note 5)		400			400		ns
	Settling Time	V_O = 20V Step (Note 4) G = 10 to 0.05% G = 10 to 0.01% G = 100 to 0.05% G = 100 to 0.01%		 1.8 3.0 7 9	 4.0 6.5 13 18		 1.8 3.0 7 9	 4.0 6.5 13 18	 µs µs µs µs

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $-55°C \le T_A \le 125°C$ for AM/M grades, $-40°C \le T_A \le 85°C$ for I grades, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM MIN	LT1102AM TYP	LT1102AM MAX	LT1102M/I MIN	LT1102M/I TYP	LT1102M/I MAX	UNITS
G_E	Gain Error	G = 100, $V_O = \pm 10V$, R_L = 50k or 2k G = 10, $V_O = \pm 10V$, R_L = 50k or 2k		0.10 0.05	0.25 0.12		0.10 0.06	0.30 0.15	% %
TCG_E	Gain Error Drift (Note 6)	G = 100, R_L = 50k or 2k G = 10, R_L = 50k or 2k		9 5	20 10		10 6	25 14	ppm/°C ppm/°C
G_{NL}	Gain Nonlinearity	G = 100, R_L = 50k G = 100, R_L = 2k G = 10, R_L = 50k or 2k		20 28 9	70 85 20		24 32 9	90 110 24	ppm ppm ppm
V_{OS}	Input Offset Voltage			300	1400		400	2000	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	µV/°C
I_{OS}	Input Offset Current			0.3	4		0.4	6	nA
I_B	Input Bias Current			±2	±10		±2.5	±15	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	82	97		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	88	100		84	99		dB
I_S	Supply Current	$T_A = 125°C$		2.5			2.5		mA
V_O	Maximal Output Voltage Swing	R_L = 50k R_L = 2k	±12.5 ±12.0	±13.2 ±12.6		±12.5 ±12.0	±13.2 ±12.6		V V

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AC MIN	LT1102AC TYP	LT1102AC MAX	LT1102C MIN	LT1102C TYP	LT1102C MAX	UNITS
G_E	Gain Error	G = 100, $V_O = \pm 10V$, R_L = 50k or 2k G = 10, $V_O = \pm 10V$, R_L = 50k or 2k		0.04 0.03	0.11 0.09		0.05 0.04	0.14 0.12	% %
TCG_E	Gain Error Drift (Note 6)	G = 100, R_L = 50k or 2k G = 10, R_L = 50k or 2k		8 5	18 10		9 6	22 14	ppm/°C ppm/°C
G_{NL}	Gain Nonlinearity	G = 100, R_L= 50k G = 100, R_L= 2k G = 10, R_L= 50k or 2k		8 11 8	30 36 18		9 12 8	40 48 22	ppm ppm ppm
V_{OS}	Input Offset Voltage			230	1000		280	1400	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	µV/°C
I_{OS}	Input Offset Current			10	150		15	220	pA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 6)		0.5	3		0.5	4	pA/°C
I_B	Input Bias Current			±40	±300		±50	±400	pA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 6)		1	4		1	6	pA/°C
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	83	98		81	97		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	87	101		85	100		dB
I_S	Supply Current	$T_A = 70°C$		2.8			2.9		mA
V_O	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±12.8 ±12.0	±13.4 ±12.8		±12.8 ±12.0	±13.4 ±12.8		V V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula:

$i_n = (2qI_B)^{1/2}$

where $q = 1.6 \bullet 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 4: This parameter is not tested. It is guaranteed by design and by inference from the slew rate measurement.

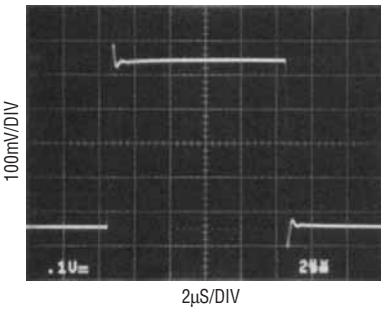
Note 5: Overdrive recovery is defined as the time delay from the removal of an input overdrive to the output's return from saturation to linear operation.

50% overdrive equals $V_{IN} = \pm 2V$ (G = 10) or $V_{IN} = \pm 200mV$ (G = 100).

Note 6: This parameter is not tested. It is guaranteed by design and by inference from other tests.

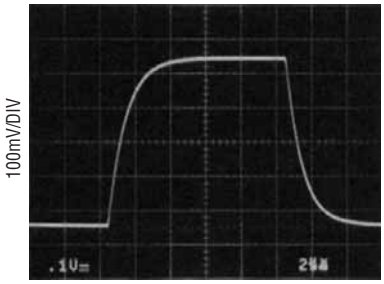
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Response, G = 10 (Input = 50mV Pulse)



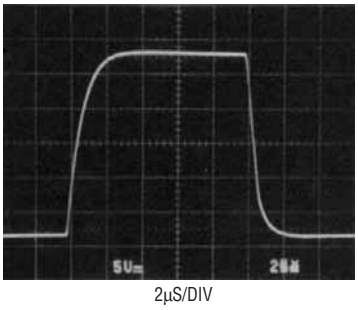
LT1102 • TPC01

Small Signal Response, G = 100 (Input = 5mV Pulse)



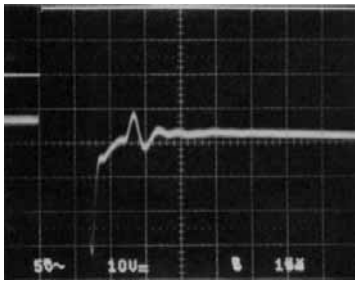
LT1102 • TPC02

Slew Rate, G = 100 (Input = ±130mV Pulse)



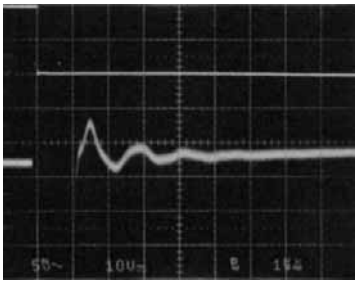
LT1102 • TPC03

Settling Time, G = 10 (Input From –10V to 10V)



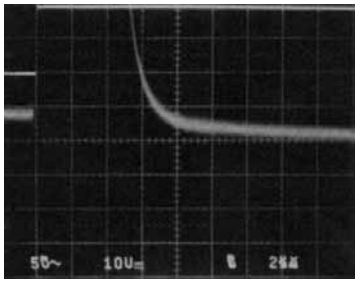
LT1102 • TPC04

Settling Time, G = 10 (Input From 10V to –10V)



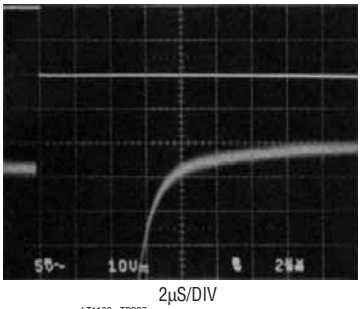
LT1102 • TPC05

Settling Time, G = 100 (Input From –10V to 10V)



LT1102 • TPC06

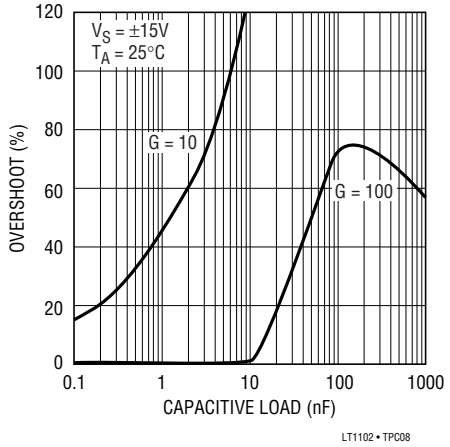
Settling Time, G = 100 (Input From 10V to –10V)



LT1102 • TPC07

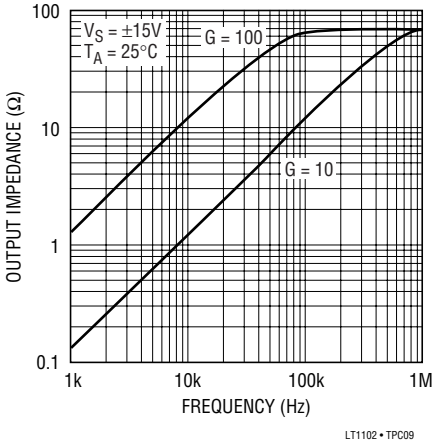
TYPICAL PERFORMANCE CHARACTERISTICS

Capacitive Load Handling



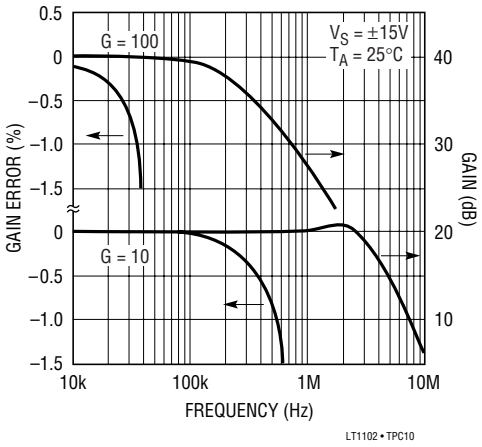
LT1102 • TPC08

Output Impedance vs Frequency



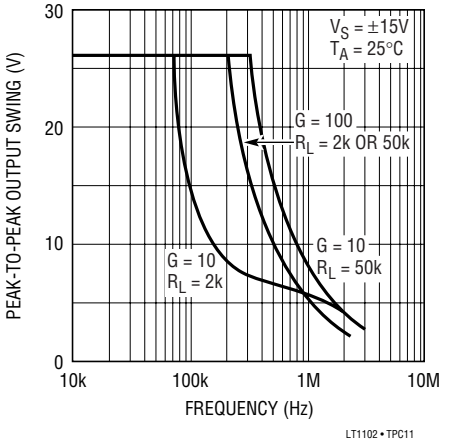
LT1102 • TPC09

Gain vs Frequency



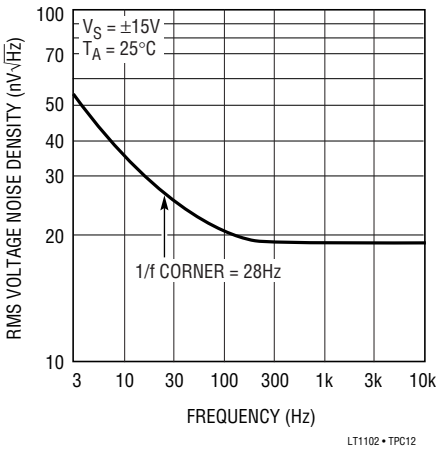
LT1102 • TPC10

Undistorted Output vs Frequency



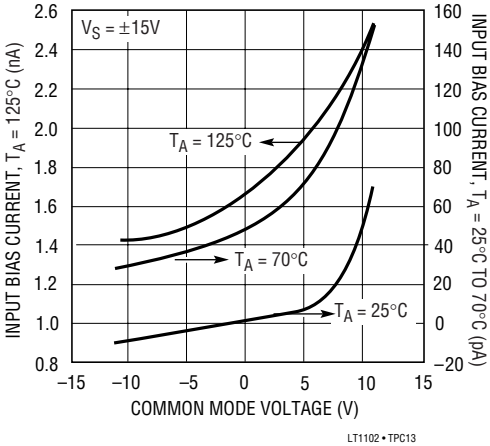
LT1102 • TPC11

Voltage Noise vs Frequency



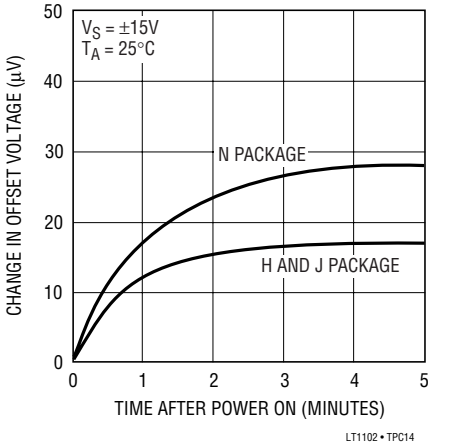
LT1102 • TPC12

Input Bias Current Over the Common Mode Range



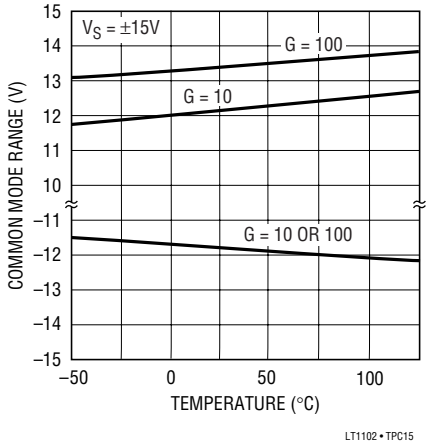
LT1102 • TPC13

Warm-Up Drift



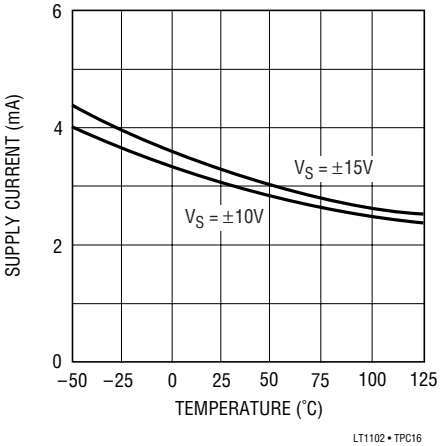
LT1102 • TPC14

Common Mode Range vs Temperature



LT1102 • TPC15

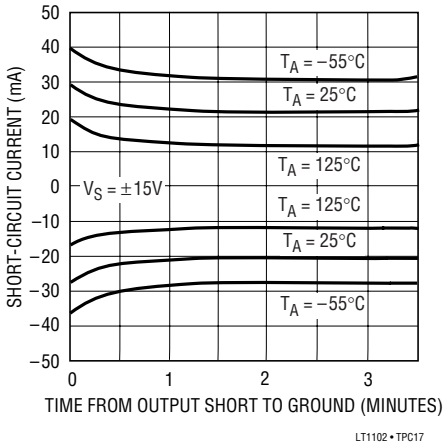
Supply Current vs Temperature



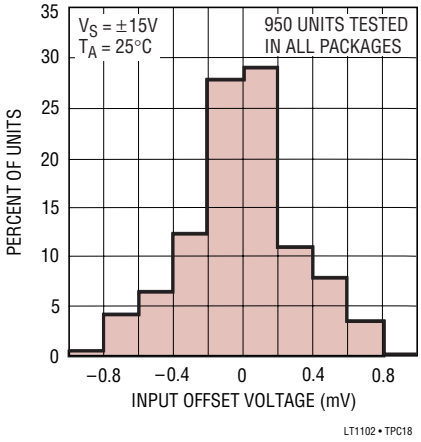
LT1102 • TPC16

TYPICAL PERFORMANCE CHARACTERISTICS

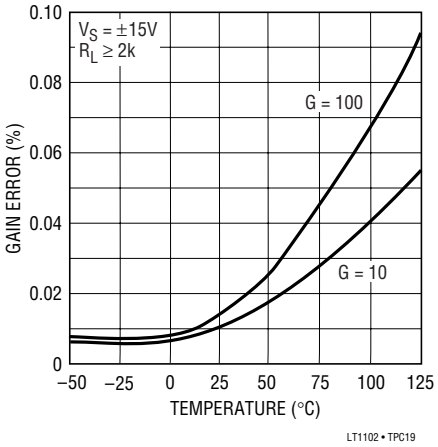
Short-Circuit Current vs Time



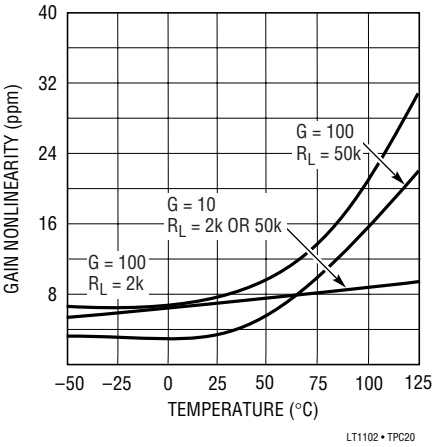
Distribution of Offset Voltage



Gain Error vs Temperature



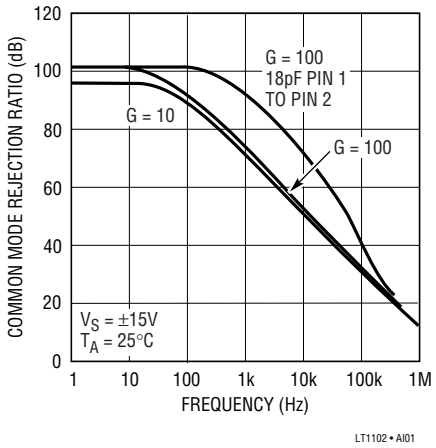
Gain Nonlinearity Over Temperature



APPLICATIONS INFORMATION

In the two op amp instrumentation amplifier configuration, the first amplifier is basically in unity gain, and the second amplifier provides all the voltage gain. In the LT1102, the second amplifier is decompensated for gain of 10 stability, therefore high slew rate and bandwidth are achieved. Common mode rejection versus frequency is also optimized in the G = 10 mode, because the bandwidths of the two op amps are similar. When G = 100, this statement is no longer true; however, by connecting an 18pF capacitor between pins 1 and 2, a common mode AC gain is created to cancel the inherent roll-off. From 200Hz to 30kHz, CMRR versus frequency is improved by an order of magnitude.

Common Mode Rejection Ratio vs Frequency



Input Protection

Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1102 employs FET input transistors, consequently the differential input voltage can be ±30V (with ±15V supplies, ±36V with ±18V supplies). Some competitive instrumentation amplifiers have NPN inputs which are protected by back-to-back diodes. When the differential input Voltage exceeds ±13V on these competitive devices, input current increases to milliampere level; more than ±10V differential voltage can cause permanent damage.

When the LT1102 inputs are pulled below the negative supply or above the positive supply, the inputs will clamp a diode voltage below or above the supplies. No damage will occur if the input current is limited to 20mA.

Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors (= R_X) between pins 1 and 2 and pins 7 and 8.

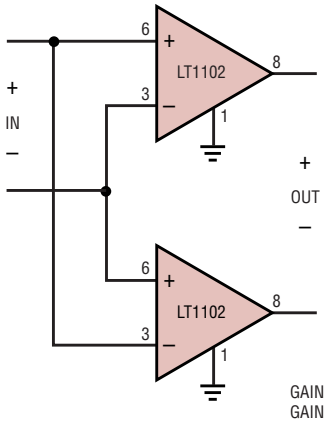
$$\text{Gain} = 10 + \frac{R_X}{R + R_X/90}$$

The nominal value of R is 1.84kΩ. The usefulness of this method is limited by the fact that R is not controlled to better than ±10% absolute accuracy in production. However, on any specific unit, 90R can be measured between Pins 1 and 2.

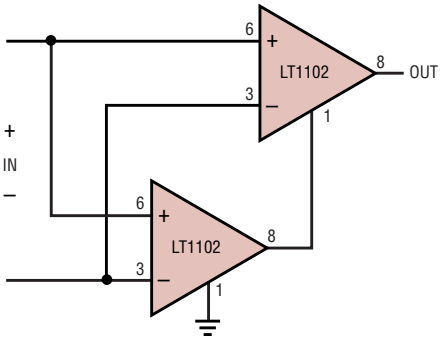
APPLICATIONS INFORMATION

Gain = 20, 110, or 200 Instrumentation Amplifiers

Differential Output



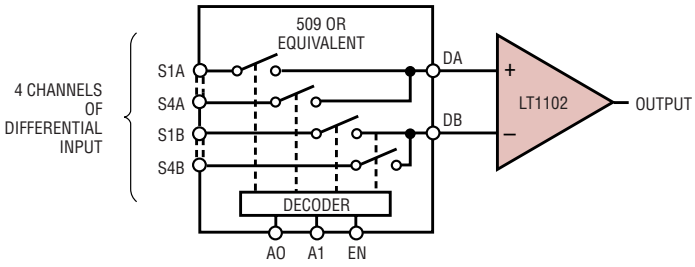
Single Ended Output



GAIN = 200, AS SHOWN
GAIN = 20, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON BOTH DEVICES
GAIN = 110, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON ONE DEVICE, NOT ON THE OTHER
INPUT REFERRED NOISE IS REDUCED BY √2 (G = 200 OR 20)

LT1102 • AI02

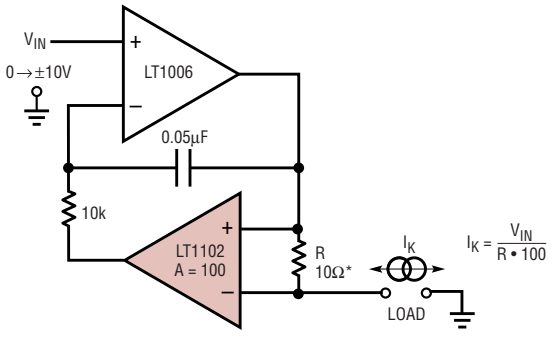
Multiplexed Input Data Acquisition



800kHz SIGNALS CAN BE MULTIPLEXED WITH LT1102 IN G = 10

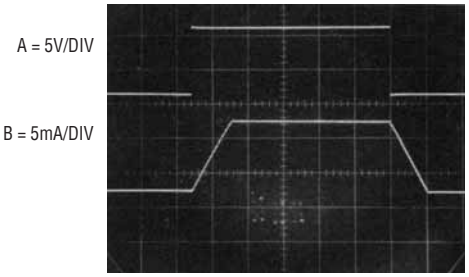
LT1102 • AI03

Voltage Programmable Current Source is Simple and Precise



LT1102 • AI04

Dynamic Response of the Current Source

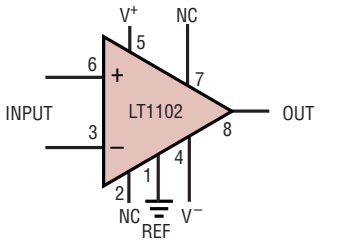


HORIZ. = 20µs/DIV

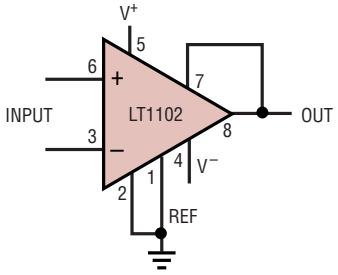
LT1102 • AI05

TYPICAL APPLICATIONS

Basic Connections



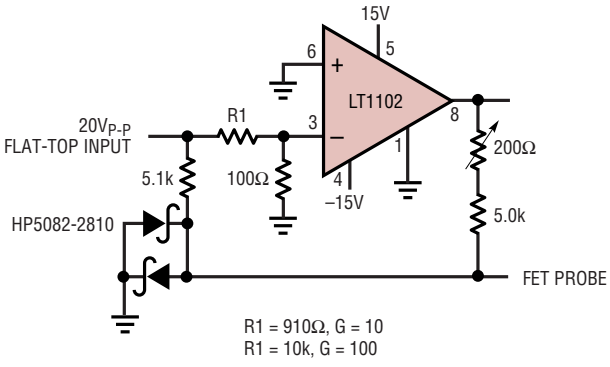
GAIN = 100



GAIN = 10

LT1102 • TA03

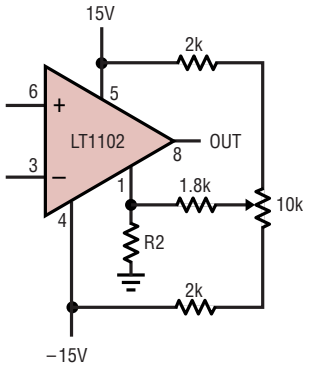
Settling Time Test Circuit



R1 = 910Ω, G = 10
R1 = 10k, G = 100

LT1102 • TA04

Offset Nulling

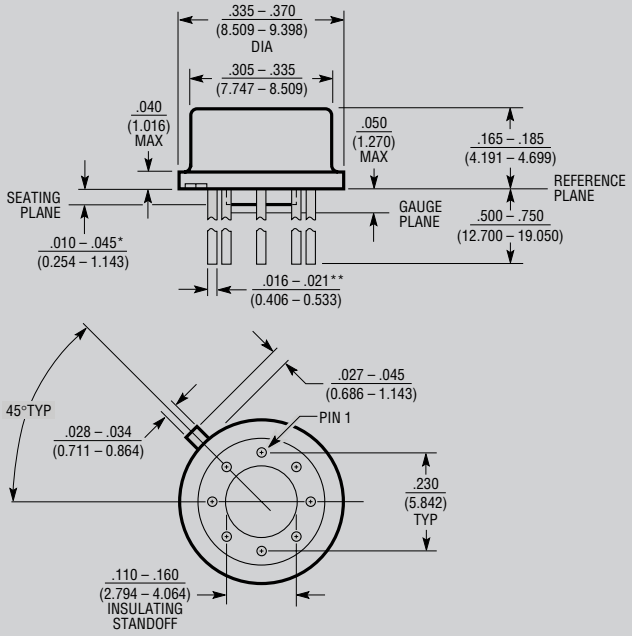


R2 = 3.3Ω, G = 10
R2 = 30Ω, G = 100
NULL RANGE = ±1mV
GAIN DEGRADATION ≈ 0.018%

LT1102 • TA05

PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.230 Inch PCD)
(Reference LTC DWG # 05-08-1321)

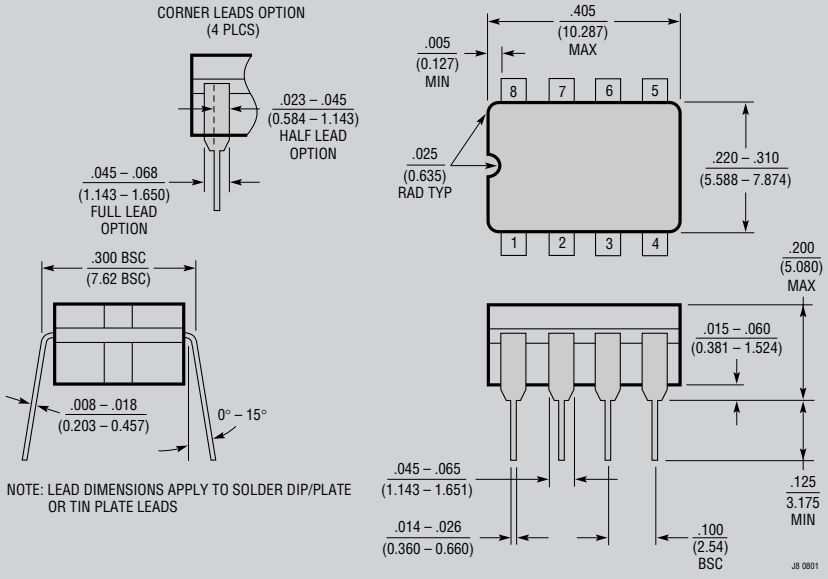


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS .016 – .024 (0.406 – 0.610)

H8 (TO-5) 0.230 PCD 0801

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

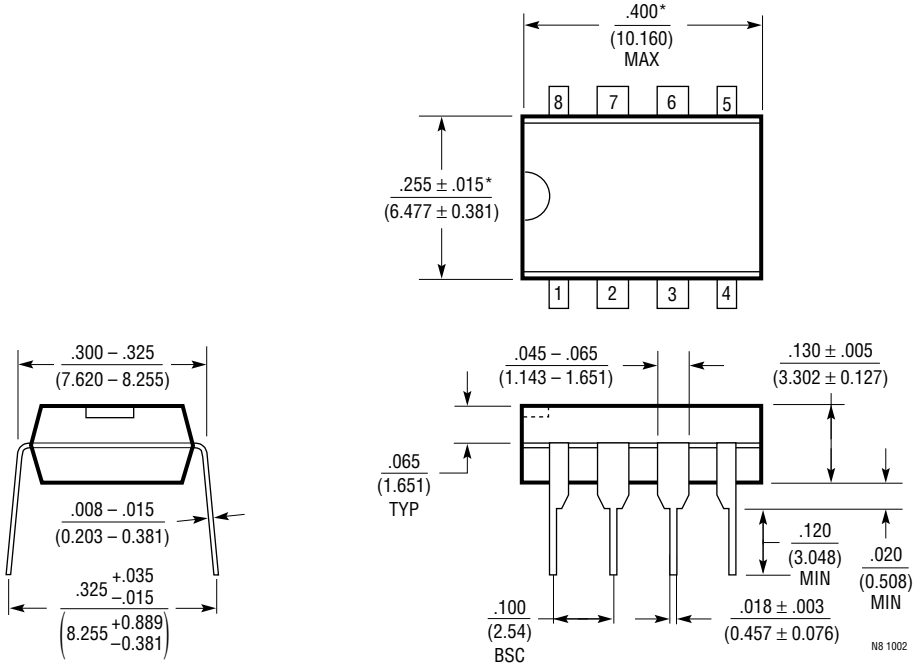


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

OBSOLETE PACKAGES

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

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