Ultra-Low Noise, Precision
OPERATIONAL AMPLIFIERS

FEATURES
- LOW NOISE: 4.5nV/√Hz max at 1kHz
- LOW OFFSET: 100µV max
- LOW DRIFT: 0.4µV/°C
- HIGH OPEN-LOOP GAIN: 117dB min
- HIGH COMMON-MODE REJECTION: 100dB min
- HIGH POWER-SUPPLY REJECTION: 94dB min
- FITS OP-07, OP-05, AD510, AND AD517 SOCKETS

APPLICATIONS
- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIERS
- RADIATION HARD EQUIPMENT

DESCRIPTION
The OPA27 and OPA37 are ultra-low noise, high-precision monolithic operational amplifiers.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full –40°C to +85°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Texas Instruments’ OPA27 and OPA37 are improved replacements for the industry-standard OP-27 and OP-37.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage ........................................... ±22V
Internal Power Dissipation (2) .......................... 500mW
Input Voltage .............................................. ±VCC
Output Short-Circuit Duration (3) ......................... Indefinite
Differential Input Voltage (4) .......................... ±0.7V
Differential Input Current (4) .......................... ±25mA
Storage Temperature Range .............................. –55°C to +125°C
Operating Temperature Range ............................ –40°C to +85°C
Lead Temperature:
P (soldering, 10s) ......................................... +300°C
U (soldering, 3s) ......................................... +260°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Maximum package power dissipation versus ambient temperature. (2) To common with ±VCC = 15V. (4) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

PACKAGE/ORDERING INFORMATION(1)

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE-LEAD</th>
<th>θJA</th>
<th>PACKAGE DRAWING</th>
<th>PACKAGE MARKING</th>
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<td>OPA27</td>
<td>DIP-8</td>
<td>100°C/W</td>
<td>P</td>
<td>OPA27GP</td>
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<tr>
<td>OPA27</td>
<td>SO-8</td>
<td>160°C/W</td>
<td>D</td>
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<td>100°C/W</td>
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<td>SO-8</td>
<td>160°C/W</td>
<td>D</td>
<td>OPA37U</td>
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</table>

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View

Offset Trim 1 2 3 4 5 6 7 8 Offset Trim
–In +In –VCC +VCC Output NC

NC = No Connection
At $V_{CC} = \pm 15\text{V}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.

### ELECTRICAL CHARACTERISTICS

#### PARAMETER | CONDITIONS | OPA27 | OPA37 | MIN | TYP | MAX | UNITS
---|---|---|---|---|---|---|---
INPUT NOISE
| Voltage, $f_O = 10\text{Hz}$ | 3.8 | 8.0 | nV/√Hz
| $f_O = 30\text{Hz}$ | 3.3 | 5.6 | nV/√Hz
| $f_O = 1\text{kHz}$ | 3.2 | 4.5 | nV/√Hz
| $f_B = 0.1\text{Hz}$ to $10\text{Hz}$ | 0.09 | 0.25 | µV/√Hz
| Current, $(1) f_O = 10\text{Hz}$ | 1.7 | | pA/√Hz
| $f_O = 30\text{Hz}$ | 1.0 | | pA/√Hz
| $f_O = 1\text{kHz}$ | 0.4 | 0.6 | pA/√Hz

OFFSET VOLTAGE
| Average Drift $(3)$ | $T_A_{MIN}$ to $T_A_{MAX}$ | ±25 | ±100 | µV
| Long Term Stability $(4)$ | 0.4 | 2.0 | µV/°C
| Supply Rejection | ±$V_{CC} = 4$ to $18\text{V}$ | 94 | 120 | dB
| | ±$V_{CC} = 4$ to $18\text{V}$ | ±1 | ±20 | µV/V

BIAS CURRENT
| Input Bias Current | ±15 | ±80 | nA

OFFSET CURRENT
| Input Offset Current | 10 | 75 | nA

IMPEDEANCE
| Common-Mode | 2 || 2.5 | GΩ || pF

VOLTAGE RANGE
| Common-Mode Input Range | ±11 | ±12.3 | V
| Common-Mode Rejection | 100 | 122 | dB

OPEN-LOOP VOLTAGE GAIN, DC
| $R_L \geq 2k\Omega$ | 117 | 124 | dB
| $R_L \geq 1k\Omega$ | 124 | | dB

FREQUENCY RESPONSE
| Gain-Bandwidth Product $(5)$ | OPA27 | 5 $(6)$ | 8 | MHz
| | OPA37 | 45 $(6)$ | 63 | MHz
| Slew Rate $(5)$ | $V_O = \pm 10\text{V}$, $R_L = 2k\Omega$ | OPA27, $G = +1$ | 1.7 $(6)$ | 1.9 | V/µs
| | OPA37, $G = +5$ | 11 $(6)$ | 11.9 | V/µs
| Settling Time, 0.01% | OPA27, $G = +1$ | 25 | µs
| | OPA37, $G = +5$ | 25 | µs

RATED OUTPUT
| Voltage Output | $R_L \geq 2k\Omega$ | ±12 | ±13.8 | V
| | $R_L \geq 600\Omega$ | ±10 | ±12.8 | V
| Output Resistance | DC, Open Loop | 70 | | Ω
| Short Circuit Current | $R_L = 0\Omega$ | 25 | 60 $(6)$ | mA

POWER SUPPLY
| Rated Voltage | | | | VDC
| Voltage Range, | | | | VDC
| | | | | VDC
| Current, Quiescent | $I_Q = 0\text{mA}$ | ±4 | ±22 | mA

TEMPERATURE RANGE
| Specification | −40 | | 85 | ºC
| Operating | −40 | | 85 | ºC

**NOTES:** (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specification are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter specified by design.
At $V_{CC} = \pm 15V$ and $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

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<td>Input Offset Voltage</td>
<td>$T_A_{MIN}$ to $T_A_{MAX}$</td>
<td>$\leq 48$</td>
<td>$\leq 220$&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>$\mu V$</td>
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<tr>
<td>Average Drift</td>
<td>$\pm V_{CC} = 4.5$ to $18V$</td>
<td>$\pm 0.4$</td>
<td>$\pm 1.8$&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>$\mu V/^\circ C$</td>
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<td>Supply Rejection</td>
<td>$\pm V_{CC} = 4.5$ to $18V$</td>
<td>90&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>122</td>
<td>dB</td>
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<td><strong>BIAS CURRENT</strong></td>
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<tr>
<td>Input Bias Current</td>
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<td>$\pm 21$</td>
<td>$\pm 150$&lt;sup&gt;(3)&lt;/sup&gt;</td>
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<tr>
<td>Input Offset Current</td>
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<td>20</td>
<td>135&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>nA</td>
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<td>Common-Mode Input Range</td>
<td>$V_N = \pm 11V_{DC}$</td>
<td>$\leq 10.5$&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>$\leq 11.8$</td>
<td>V</td>
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<td>Common-Mode Rejection</td>
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<td>96&lt;sup&gt;(3)&lt;/sup&gt;</td>
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<td>Open-Loop Voltage Gain</td>
<td>$R_L \geq 2k\Omega$</td>
<td>113&lt;sup&gt;(3)&lt;/sup&gt;</td>
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<tr>
<td>Voltage Output</td>
<td>$R_L = 2k\Omega$, $V_O = 0V_{DC}$</td>
<td>$\leq 11.0$&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>$\leq 13.4$</td>
<td>V</td>
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<td>Short Circuit Current</td>
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<td>mA</td>
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<td>$-40$</td>
<td>$+85$</td>
<td>$^\circ C$</td>
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</tbody>
</table>

**NOTES:** (1) Offset voltage specification are measured with automatic test equipment after approximately 0.5s from power turn-on. (2) Unnulled or nulled with 8k$\Omega$ to 20k$\Omega$ potentiometer. (3) This parameter specified by design.
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ C$, $\pm V_{CC} = \pm 15V_{DC}$, unless otherwise noted.

**INPUT OFFSET VOLTAGE WARM-UP DRIFT**

- Time From Power Turn-On (min)
- Offset Voltage Change (µV)

**INPUT VOLTAGE NOISE vs NOISE BANDWIDTH**

- Noise Bandwidth (Hz)
- Voltage Noise (µVrms)

**TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY**

- Source Resistance (Ω)
- Voltage Noise (nV/√Hz)

**VOLTAGE NOISE SPECTRAL DENSITY vs TEMPERATURE**

- Ambient Temperature (°C)
- Voltage Noise (nV/√Hz)

**VOLTAGE NOISE SPECTRAL DENSITY vs SUPPLY VOLTAGE**

- Supply Voltage (V$_{CC}$)
- Voltage Noise (nV/√Hz)

**INPUT CURRENT NOISE SPECTRAL DENSITY**

- Frequency (Hz)
- Current Noise (pA/√Hz)

**Warning:** This industry-standard equation is inaccurate and these figures should be used for comparison purposes only!
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $\pm V_{CC} = \pm 15V_{DC}$, unless otherwise noted.
TYPICAL CHARACTERISTICS (Cont.)

At $T_a = +25^\circ C$, $\pm V_{CC} = \pm 15VDC$, unless otherwise noted.

**POWER SUPPLY REJECTION vs FREQUENCY**

- $V_{CC}$ = 120dB
- Frequency (Hz)

**OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE**

- $R_L = 2k\Omega$
- $R_{L} = 600\Omega$

**OPEN-LOOP VOLTAGE GAIN vs TEMPERATURE**

- Ambient Temperature ($°C$)

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

- Supply Voltage (V$_{CC}$)

**COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE**

- Common-Mode Range (V)

**OPA27 SMALL SIGNAL TRANSIENT RESPONSE**

- Output Voltage (mV)

- Time ($\mu$s)

- $A_{VCL} = +1$
- $C_L = 15pF$
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ C$, $\pm V_{CC} = \pm 15VDC$, unless otherwise noted.

**OPA37 SMALL SIGNAL TRANSIENT RESPONSE**

<table>
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<tr>
<th>Time (µs)</th>
<th>0</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
<th>1.2</th>
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<tr>
<td>Output Voltage (mV)</td>
<td>0</td>
<td>0.2</td>
<td>0.4</td>
<td>0.6</td>
<td>0.8</td>
<td>1.0</td>
<td>1.2</td>
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$A_V = +5$
$C_L = 25pF$

**OPA27 LARGE SIGNAL TRANSIENT RESPONSE**

<table>
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<tr>
<th>Time (µs)</th>
<th>0</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
<th>10</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage (V)</td>
<td>-6</td>
<td>-4</td>
<td>-2</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>6</td>
</tr>
</tbody>
</table>

$A_{VCL} = +1$

**OPA37 LARGE SIGNAL TRANSIENT RESPONSE**

<table>
<thead>
<tr>
<th>Time (µs)</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
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<tbody>
<tr>
<td>Output Voltage (V)</td>
<td>-15</td>
<td>-10</td>
<td>-5</td>
<td>0</td>
<td>5</td>
<td>10</td>
<td>15</td>
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</tbody>
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$A_V = +5$
OFFSET VOLTAGE ADJUSTMENT

The OPA27 and OPA37 offset voltages are laser-trimmed and require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used, but $V_{OS}$ drift will be degraded by an additional 0.1µV/°C to 0.2µV/°C. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 3.3µV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27 and OPA37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

THERMOELECTRIC POTENTIALS

The OPA27 and OPA37 are laser-trimmed to microvolt-level input offset voltages, and for very-low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMFs if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference (see Figure 11).

Short, direct mounting of the OPA27 and OPA37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

**FIGURE 1.** 0.1Hz to 10Hz Noise Test Circuit.

**FIGURE 2.** Low Frequency Noise.
NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ, the OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27, as shown in Figure 5.

![Offset Voltage Trim](image1)

**FIGURE 3. Offset Voltage Trim.**

![High Resolution Offset Voltage Trim](image2)

**FIGURE 4. High Resolution Offset Voltage Trim.**

![Voltage Noise Spectral Density Versus Source Resistance](image3)

**FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.**

COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_F) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_F and C_IN and eliminate peaking or oscillation.

INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27 and OPA37. Exceeding a few hundred millivolts differential input signal will cause current to flow, and without external current limiting resistors, the input will be destroyed. Accidental static discharge, as well as high current, can damage the amplifier’s input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged, as will any precision operational amplifier subjected to this abuse.

Transient conditions can cause feedthrough due to the amplifier’s finite slew rate. When using the OPA27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended, as shown in Figure 6.

![Pulsed Operation](image4)

**FIGURE 6. Pulsed Operation.**

![Low-Noise RIAA Preamplifier](image5)

**FIGURE 7. Low-Noise RIAA Preamplifier.**

![Unity-Gain Inverting Amplifier](image6)

**FIGURE 8. Unity-Gain Inverting Amplifier.**
FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

FIGURE 10. NAB Tape Head Preamplifier.

FIGURE 11. Low Frequency Noise Comparison.

A. 741 noise with circuit well-shielded from air currents and RFI. (Note scale change.)

B. OP-07AH with circuit well-shielded from air currents and RFI.

C. OPA27AJ with circuit well-shielded from air currents and RFI. (Represents ultimate OPA27 performance potential.)

D. OPA27 with circuit unshielded and exposed to normal lab bench-top air currents. (External thermoelectric potentials far exceed OPA27 noise.)

E. OPA27 with heat sink and shield which protects input leads from air currents. Conditions same as (D).
FIGURE 12. Low Noise Instrumentation Amplifier.

FIGURE 13. Hydrophone Preamplifier.


FIGURE 15. High Performance Synchronous Demodulator.

Gain = –1010 V/V

$V_{OS} = 2\mu V$

Drift = 0.07\mu V/°C

$e_n = 1nV/\sqrt{Hz}$ at 10Hz

$0.9nV/\sqrt{Hz}$ at 100Hz

$0.87nV/\sqrt{Hz}$ at 1kHz

Full Power Bandwidth = 180kHz

Gain Bandwidth = 500MHz

Equivalent Noise Resistance = 50Ω

Signal-to-Noise Ratio ∝ $\sqrt{N}$ since amplifier noise is uncorrelated.
FIGURE 17. Unity-Gain Buffer.

FIGURE 18. High Slew Rate Unity-Gain Buffer.

FIGURE 19. RF Detector and Video Amplifier.


\[ f_{\text{OUT}} = \text{RPM} \cdot N \]

Where \( N \) = Number of Gear Teeth
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
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<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
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<td>RoHS &amp; Green</td>
<td>NIPDAU-DCC</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>OPA37U</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (W1) (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA27GU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA37GU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA27GU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA37GU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.