Instrumentation amplifiers, load-cell amplification, a review of the experiment, current measurement and some current sources.

Week 7: AoE 7.09-7.12; 15.03

Keithley low-level measurements handbook
The Wheatstone bridge

Suppose we have a constant $V$ bridge excitation. Then the total current passing through the bridge is:

$$I_{tot} = \frac{V}{(R_A + R_B)||(R_C + R_D)}$$

For simplicity, and to get an idea of how this bridge works, let’s assume that both dividers have an equal resistance, and furthermore that all resistor values are identical. Then $\Delta V = 0$.

Now, consider a case where $R_A$ increases by an amount $dR$, and $R_D$ decreases by $dR$. In this case, the current passing through the two halves of the bridge (each a divider!) is no longer identical. In fact, the left current is: $V/(R_A + dR + R_B)$, while the right current is $V/(R_C + R_D - dR)$.

Thus, the voltage on the left is $R_B * V / (R_A + dR + R_B)$, and on the right, $(R_D - dR)*V/(R_C + R_D - dR)$, and after a significant amount of algebra, we find to leading order that $\Delta V \sim 2 dR$ (the exact calculation you can do if you like!)

Fundamentally, this circuit becomes non-linear when $dR$ becomes large compared with all the $R$ in the bridge.
A load-cell circuit consisting of strain gages in the Wheatstone-bridge configuration:

Upon application of force, $F$, the strain gauges respond by changing their resistance. Under compression, the resistance decreases; under tension, the resistance increases.

Thus we can quickly see that the differential voltage will systematically change in response to applied force, as the $v$-dividers formed by the strain gauges in each side of the load cell will change their primary voltage values in a levered-fashion.

Nevertheless, the mean value sits around 5 V!

For discussion on Piazza: why would one wish to ensure that the resistors in each leg see the same amount of current, as is achieved by this bridge configuration?
Often we are tasked with the measurement of a transducer’s output.

The main challenge addressed by instrumentation amplifiers is high rejection of common-mode voltage (CMRR).

The high CMRR is necessary because often transducers (such as load cells) have high common-mode signals (of order several V), while the signal of interest is a differential signal in the mV-scale.

If we want a 0.1% accuracy of a mV signal, say, then we must reject 5 V-common-mode down to the microvolt level (!) this corresponds to a rejection of over a million times the common-mode!

How can we achieve this?
The previous circuit should look familiar from the handout on instrumentation amplifiers. These are useful devices for discarding common-mode signals!

A word of caution on CMRR in INAs: see from the INA 122 datasheet:

\textit{CMRR drops at high-frequency!}
The bulk resistivity of aluminum is \( \sim 2.8 \times 10^{-8} \) Ohm.meters. The coating thickness is ca. 30 nm, the sample is 5 cm wide, and the gage between conductors is ca. 5 cm. You can thus estimate \( R_{\text{alu}} \); if it is less than 100 Ohm, 4 wire is needed!
Exercises this week:

1. Measure the resistance of an uncracked sample -> 4-wire method. Use copper strips to ensure you’re measuring across the whole coating.

2. Measure the ‘cracked’ sample to get an idea of the range of R you should expect.

3. Design your Wheatstone bridge, specifying the values of R in the other legs. Build a voltage source for the bridge (bridge `excitation’). Keep in mind the power dissipated by the bridge!

4. Come up with a way to measure crack length and velocity based on the resistance of the plate and your bridge architecture. Can you do both? How? I’ll briefly introduce some helpful amplifiers / circuits now.
Voltage sources & current sources: REF 102
A new arrival: high-GBP instrumentation amp, LT1102
A fast, non-unity gain-stable op-amp: OPA 37
10V Precision Voltage Reference

FEATURES

- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5µVpp typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: PLASTIC DIP, SO-8

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETER
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max C-grade over the industrial temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single-supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.
ABSOLUTE MAXIMUM RATINGS(1)

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<th>PACKAGE DESIGNATOR</th>
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<td>±10</td>
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NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

PIN CONFIGURATIONS

Top View

- NC = Not Connected
- Noise Reduction
- V+ 2
- NC 3
- Com 4
- VOUT 6
- Trim 5
- NC 7

DIP, SO

---

NC = Not Connected
### ELECTRICAL CHARACTERISTICS

At $T_A = +25^\circ C$ and $V_S = +15V$ power supply, unless otherwise noted.

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<td>vs Time</td>
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<td>$I_{OUT} = 0$</td>
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<td>+36</td>
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<td>*</td>
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* Specifications same as REF102A.

**NOTES:**
1. (1) The box method is used to specify output voltage drift vs temperature; see the Discussion of Performance section.
2. (2) Typically 5ppm/1000hrs after 168hr powered stabilization.
3. (3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details.
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ$C, $V_S = +15V$, unless otherwise noted.

**POWER TURN-ON RESPONSE**

- $V_{OUT}$ vs $V_{IN}$
- Time (5µs/div)

**POWER TURN-ON RESPONSE with 1µF $C_N$**

- $V_{OUT}$ vs $V_{IN}$
- Time (10ms/div)

**POWER SUPPLY REJECTION vs FREQUENCY**

- Frequency (Hz) vs Power Supply Rejection (dB)

**LOAD REGULATION**

- Output Current (mA) vs Output Voltage Change (mV)

**RESPONSE TO THERMAL SHOCK**

- Time (s) vs Output Voltage Change (µV)

**QUIESCENT CURRENT vs TEMPERATURE**

- Temperature (°C) vs Quiescent Current (mA)
TYPICAL CHARACTERISTICS (Cont.)

At $T_a = +25^\circ$C, $V_S = +15$V, unless otherwise noted.

![Typical REF102 Reference Noise](image)

**TYPICAL REF102 REFERENCE NOISE**

Noise Voltage (µV)

Low Frequency Noise (1s/div)

(See Noise Test Circuit)

**THEORY OF OPERATION**

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode $DZ_1$, op amp $A_1$, and resistor network $R_1 - R_6$. Approximately 8.2V is applied to the non-inverting input of $A_1$ by $DZ_1$. $R_1$, $R_2$, and $R_3$ are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through $R_4$. $R_5$ allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the temperature coefficient (TCR) of $R_5$ closely matches the TCR of $R_1$, $R_2$ and $R_3$, the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with $R_6$ and roll off the high-frequency noise of the zener.

**DISCUSSION OF PERFORMANCE**

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the butterfly method and the box method. The REF102 is specified by the more commonly-used box method. The box is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not known, either. It is, however, bounded by $V_{\text{UPPER BOUND}}$ and $V_{\text{LOWER BOUND}}$ (see Figure 1). Figure 1 uses the REF102CU as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of $-25^\circ$C to $+85^\circ$C. The box height, $V_1$ to $V_2$, is 2.75mV.

![Figure 1. REF102CU Output Voltage Drift](image)
INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated, being sure to minimize interconnection resistances.

![Figure 2. REF102 Installation.](image1)

NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between $R_S$ and the internal resistors can introduce some slight drift. This effect is minimized if $R_S$ is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

![Figure 3. REF102 Optional Output Voltage Adjust.](image2)

![Figure 4. REF102 Optional Output Voltage, Fine Adjust.](image3)
OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low-pass filter with \( R_6 \) (refer to the figure on page 1) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1\( \mu \)F noise reduction capacitor on the high-frequency noise of the REF102. \( R_6 \) is typically 7k\( \Omega \) so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about 800\( \mu \)VP-P to under 200\( \mu \)VP-P. If further noise reduction is required, use the circuit in Figure 14.

![Image](image.png)

FIGURE 5. Effect of 1\( \mu \)F Noise Reduction Capacitor on Broadband Noise (\( f_{-3dB} = 1MHz \))

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

![Image](image2.png)

FIGURE 6. –10V Reference Using a) Resistor or b) OPA227.

See SBVA008 for more detail.
FIGURE 7. +10V Reference With Output Current Boosted to: a) $-20mA < I_L < +20mA$
  (OPA227 also improves transient immunity), b) $-5mA < I_L < +100mA$, and c) $I_L(TYP) +10mA$, $-5A$.

FIGURE 8. Strain Gauge Conditioner for 350$\Omega$ Bridge.

FIGURE 9. ±10V Reference.

FIGURE 10. Positive Precision Current Source.
NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between $10n + 1.4$ and $10n + 26$, where $n$ is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of $+10$, $-5mA$. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

FIGURE 12. ±5V Reference.

FIGURE 13. +5V and +10V Reference.


$\sqrt{N}$

$\frac{v_{REF} = (v_{V1} + v_{V2} \ldots v_{V_{OUT} \ldots})}{N}$

$e_n = 5\sqrt{v_{pp}}$ ($f = 0.1Hz$ to $1MHz$)

See SBVA002 for more details.
## Revision History

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<th>DATE</th>
<th>REVISION</th>
<th>PAGE</th>
<th>SECTION</th>
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<td>B</td>
<td>2</td>
<td>Absolute Maximum Ratings</td>
<td>Deleted lead temperature rating.</td>
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<td>Package/Ordering Information</td>
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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
## PACKAGING INFORMATION

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<th>MSL Peak Temp (3)</th>
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<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-25 to 85</td>
<td>Samples</td>
<td></td>
</tr>
<tr>
<td>REF102CU/2K5</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-25 to 85</td>
<td>Samples</td>
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<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-25 to 85</td>
<td>Samples</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<tbody>
<tr>
<td>REF102AU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
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<tr>
<td>REF102CU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
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<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF102AU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
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<tr>
<td>REF102CU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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The LT1102 is the first fast FET input instrumentation amplifier offered in the low cost, space saving 8-pin packages. Fixed gains of 10 and 100 are provided with excellent gain accuracy (0.01%) and non-linearity (3ppm). No external gain setting resistor is required.

Slew rate, settling time, gain-bandwidth product, overdrive recovery time are all improved compared to competitive high speed instrumentation amplifiers.

Industry best speed performance is combined with impressive precision specifications: less than 10pA input bias and offset currents, 180μV offset voltage. Unlike other FET input instrumentation amplifiers, on the LT1102 there is no output offset voltage contribution to total error, and input bias currents do not double with every 10°C rise in temperature. Indeed, at 70°C ambient temperature the input bias current is only 40pA.

**FEATURES**
- Slew Rate: 30V/μs
- Gain-Bandwidth Product: 35MHz
- Settling Time (0.01%): 3μs
- Overdrive Recovery: 0.4μs
- Gain Error: 0.05% Max
- Gain Drift: 5ppm/°C
- Gain Nonlinearity: 16ppm Max
- Offset Voltage (Input + Output): 600μV Max
  - Drift with Temperature: 2μV/°C
- Input Bias Current: 40pA Max
- Input Offset Current: 40pA Max
  - Drift with Temperature (to 70°C): 0.5pA/°C

**APPLICATIONS**
- Fast Settling Analog Signal Processing
- Multiplexed Input Data Acquisition Systems
- High Source Impedance Signal Amplification from High Resistance Bridges, Capacitance Sensors, Photodetector Sensors
- Bridge Amplifier with < 1Hz Lowpass Filtering

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---

**Wideband Instrumentation Amplifier with ±150mA Output Current**

**Slew Rate**

![Slew Rate Graph](attachment:image.png)
LT1102

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage ...................................................... ±20V
Differential Input Voltage .................................... ±40V
Input Voltage ........................................................ ±20V

Output Short-Circuit Duration .......................... Indefinite
Operating Temperature Range
  LT1102I .............................................. –40°C to 85°C
  LT1102AC/LT1102C ................................ 0°C to 70°C
  LT1102AM/LT1102M (OBSOLETE).....–55°C to 125°C
Storage Temperature Range .......................... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ............... 300°C

**ORDER OPTIONS**
- Tape and Reel: Add #TR
- Lead Free: Add #PBF
- Lead Free Tape and Reel: Add #TRPBF

Consult LTC Marketing for parts specified with wider operating temperature ranges.
## ELECTRICAL CHARACTERISTICS

$V_S = \pm 15\,V$, $V_{CM} = 0\,V$, $T_A = 25^\circ C$, Gain = 10 or 100, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1102AM/AC</th>
<th>LT1102M/I/C</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_E$</td>
<td>Gain Error</td>
<td>$V_D = \pm 10,V$, $R_L = 50k$ or $2k$</td>
<td>MIN 0.010  TYP 0.050  MAX 0.070</td>
<td>MIN 0.012  TYP 0.070  MAX 0.070</td>
<td>%</td>
</tr>
<tr>
<td>$G_{NL}$</td>
<td>Gain Nonlinearity</td>
<td>$G = 100$, $R_L = 50k$</td>
<td>MIN 3  TYP 14  MAX 18</td>
<td>MIN 4  TYP 18  MAX 25</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 100$, $R_L = 2k$</td>
<td>MIN 8  TYP 20  MAX 25</td>
<td>MIN 8  TYP 25  MAX 30</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$, $R_L = 50k$ or $2k$</td>
<td>MIN 7  TYP 16  MAX 30</td>
<td>MIN 7  TYP 30  MAX 30</td>
<td>ppm</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>Input Offset Voltage</td>
<td>180  600</td>
<td>200  900</td>
<td>µV</td>
<td></td>
</tr>
<tr>
<td>$I_{DS}$</td>
<td>Input Offset Current</td>
<td>3  40</td>
<td>4  60</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Input Bias Current</td>
<td>±3  ±40</td>
<td>±4  ±60</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Resistance</td>
<td>$V_{CM} = 0,V$</td>
<td>$10^{12}$  $10^{12}$  $10^{12}$</td>
<td>$10^{12}$  $10^{12}$  $10^{12}$</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Common Mode</td>
<td>$V_{CM} = \pm 11,V$ to $8,V$</td>
<td>$10^{10}$  $10^{10}$  $10^{10}$</td>
<td>$10^{10}$  $10^{10}$  $10^{10}$</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Differential Mode</td>
<td>$V_{CM} = 0,V$ to $11,V$</td>
<td>$10^{12}$  $10^{12}$  $10^{12}$</td>
<td>$10^{12}$  $10^{12}$  $10^{12}$</td>
<td>Ω</td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input Noise Voltage</td>
<td>0.1Hz to 10Hz</td>
<td>2.8  2.8</td>
<td>µVP-P</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Noise Voltage Density</td>
<td>$f_O = 10,Hz$</td>
<td>37  37</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_O = 1000,Hz$ (Note 2)</td>
<td>19  20</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>180  600</td>
<td>200  900</td>
<td>µV</td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td>3  40</td>
<td>4  60</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Bias Current</td>
<td>±3  ±40</td>
<td>±4  ±60</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>$R_{S}$</td>
<td>Input Resistance</td>
<td>$V_{CM} = \pm 11,V$ to $8,V$</td>
<td>$10^{12}$  $10^{12}$  $10^{12}$</td>
<td>$10^{12}$  $10^{12}$  $10^{12}$</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Common Mode</td>
<td>$V_{CM} = 0,V$</td>
<td>$10^{10}$  $10^{10}$  $10^{10}$</td>
<td>$10^{10}$  $10^{10}$  $10^{10}$</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Differential Mode</td>
<td>$V_{CM} = \pm 11,V$ to $8,V$</td>
<td>$10^{12}$  $10^{12}$  $10^{12}$</td>
<td>$10^{12}$  $10^{12}$  $10^{12}$</td>
<td>Ω</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common Mode Rejection Ratio</td>
<td>1k Source Imbalance, $V_{CM} = \pm 10.5,V$</td>
<td>84  98</td>
<td>82  97</td>
<td>dB</td>
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<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection Ratio</td>
<td>$V_S = \pm 9,V$ to $\pm 18,V$</td>
<td>88  102</td>
<td>86  101</td>
<td>dB</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>3.3  5.0</td>
<td>3.4  5.6</td>
<td>mA</td>
<td></td>
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<tr>
<td>$V_O$</td>
<td>Maximum Output Voltage</td>
<td>$R_L = 50k$</td>
<td>MIN ±13.0  TYP ±13.0  MAX ±13.5</td>
<td>MIN ±13.0  TYP ±13.5  MAX ±13.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Voltage Swing</td>
<td>$R_L = 2k$</td>
<td>MIN ±12.0  TYP ±13.0  MAX ±13.0</td>
<td>MIN ±12.0  TYP ±13.5  MAX ±13.5</td>
<td>V</td>
</tr>
<tr>
<td>$BW$</td>
<td>Bandwidth</td>
<td>$G = 100$ (Note 4)</td>
<td>120  220</td>
<td>100  220</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$ (Note 4)</td>
<td>2.0  3.5</td>
<td>1.7  3.5</td>
<td>MHz</td>
</tr>
<tr>
<td>$SR$</td>
<td>Slew Rate</td>
<td>$G = 100$, $V_{IN} = \pm 0.13,V$, $V_D = \pm 5,V$</td>
<td>12  17</td>
<td>10  17</td>
<td>V/µs</td>
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<td></td>
<td></td>
<td>$G = 10$, $V_{IN} = \pm 1,V$, $V_D = \pm 5,V$</td>
<td>21  30</td>
<td>18  30</td>
<td>V/µs</td>
</tr>
<tr>
<td></td>
<td>Overdrive Recovery</td>
<td>50% Overdrive (Note 5)</td>
<td>400  400</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$Settling Time$</td>
<td>$V_D = 20,V$ Step (Note 4)</td>
<td>$G = 10$ to 0.05%</td>
<td>1.8  4.0</td>
<td>1.8  4.0</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$ to 0.01%</td>
<td>3.0  6.5</td>
<td>3.0  6.5</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 100$ to 0.05%</td>
<td>7  13</td>
<td>7  13</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 100$ to 0.01%</td>
<td>9  18</td>
<td>9  18</td>
<td>µs</td>
</tr>
</tbody>
</table>
### LT1102

#### Electrical Characteristics

For AM/M grades, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for I grades, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1102AM</th>
<th>LT1102M/I</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_E$</td>
<td>Gain Error</td>
<td>$G = 100$, $V_O = \pm 10\text{V}$, $R_L = 50k$ or $2k$</td>
<td>0.10 0.25</td>
<td>0.10 0.30</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$, $V_O = \pm 10\text{V}$, $R_L = 50k$ or $2k$</td>
<td>0.05 0.12</td>
<td>0.06 0.15</td>
<td>%</td>
</tr>
<tr>
<td>$TCG_E$</td>
<td>Gain Error Drift (Note 6)</td>
<td>$G = 100$, $R_L = 50k$ or $2k$</td>
<td>9 20</td>
<td>10 25</td>
<td>ppm/°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$, $R_L = 50k$ or $2k$</td>
<td>5 10</td>
<td>6 14</td>
<td>ppm/°C</td>
</tr>
<tr>
<td>$G_{NL}$</td>
<td>Gain Nonlinearity</td>
<td>$G = 100$, $R_L = 50k$</td>
<td>20 70</td>
<td>24 90</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 100$, $R_L = 2k$</td>
<td>28 85</td>
<td>32 110</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$, $R_L = 50k$ or $2k$</td>
<td>9 20</td>
<td>9 24</td>
<td>ppm</td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td></td>
<td>300 1400</td>
<td>400 2000</td>
<td>µV</td>
</tr>
<tr>
<td>$\Delta V_{OS}/\Delta T$</td>
<td>Input Offset Voltage Drift (Note 6)</td>
<td></td>
<td>2 8</td>
<td>3 12</td>
<td>µV/°C</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td></td>
<td>0.3 4</td>
<td>0.4 6</td>
<td>nA</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td></td>
<td>±2 ±10</td>
<td>±2.5 ±15</td>
<td>nA</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common Mode Rejection Ratio</td>
<td>$V_{CM} = \pm 10.3\text{V}$</td>
<td>82 97</td>
<td>80 96</td>
<td>dB</td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection Ratio</td>
<td>$V_S = \pm 10\text{V}$ to $\pm 17\text{V}$</td>
<td>88 100</td>
<td>84 99</td>
<td>dB</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>$T_A = 125^\circ\text{C}$</td>
<td>2.5</td>
<td>2.5</td>
<td>mA</td>
</tr>
<tr>
<td>$V_O$</td>
<td>Maximum Output Voltage Swing</td>
<td>$R_L = 50k$</td>
<td>±12.5 ±13.2</td>
<td>±12.5 ±13.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 2k$</td>
<td>±12.0 ±12.6</td>
<td>±12.0 ±12.6</td>
<td>V</td>
</tr>
</tbody>
</table>

For $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, Gain = 10 or 100, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1102AC</th>
<th>LT1102C</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_E$</td>
<td>Gain Error</td>
<td>$G = 100$, $V_O = \pm 10\text{V}$, $R_L = 50k$ or $2k$</td>
<td>0.04 0.11</td>
<td>0.05 0.14</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$, $V_O = \pm 10\text{V}$, $R_L = 50k$ or $2k$</td>
<td>0.03 0.09</td>
<td>0.04 0.12</td>
<td>%</td>
</tr>
<tr>
<td>$TCG_E$</td>
<td>Gain Error Drift (Note 6)</td>
<td>$G = 100$, $R_L = 50k$ or $2k$</td>
<td>8 18</td>
<td>9 22</td>
<td>ppm/°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$, $R_L = 50k$ or $2k$</td>
<td>5 10</td>
<td>6 14</td>
<td>ppm/°C</td>
</tr>
<tr>
<td>$G_{NL}$</td>
<td>Gain Nonlinearity</td>
<td>$G = 100$, $R_L = 50k$</td>
<td>8 30</td>
<td>9 40</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 100$, $R_L = 2k$</td>
<td>11 36</td>
<td>12 48</td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$G = 10$, $R_L = 50k$ or $2k$</td>
<td>8 18</td>
<td>8 22</td>
<td>ppm</td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td></td>
<td>230 1000</td>
<td>280 1400</td>
<td>µV</td>
</tr>
<tr>
<td>$\Delta V_{OS}/\Delta T$</td>
<td>Input Offset Voltage Drift (Note 6)</td>
<td></td>
<td>2 8</td>
<td>3 12</td>
<td>µV/°C</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
<td></td>
<td>10 150</td>
<td>15 220</td>
<td>pA</td>
</tr>
<tr>
<td>$\Delta I_{OS}/\Delta T$</td>
<td>Input Offset Current Drift (Note 6)</td>
<td></td>
<td>0.5 3</td>
<td>0.5 4</td>
<td>pA/°C</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current</td>
<td></td>
<td>±40 ±300</td>
<td>±50 ±400</td>
<td>pA</td>
</tr>
<tr>
<td>$\Delta I_B/\Delta T$</td>
<td>Input Bias Current Drift (Note 6)</td>
<td></td>
<td>1 4</td>
<td>1 6</td>
<td>pA/°C</td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common Mode Rejection Ratio</td>
<td>$V_{CM} = \pm 10.3\text{V}$</td>
<td>83 98</td>
<td>81 97</td>
<td>dB</td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power Supply Rejection Ratio</td>
<td>$V_S = \pm 10\text{V}$ to $\pm 17\text{V}$</td>
<td>87 101</td>
<td>85 100</td>
<td>dB</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>$T_A = 70^\circ\text{C}$</td>
<td>2.8</td>
<td>2.9</td>
<td>mA</td>
</tr>
<tr>
<td>$V_O$</td>
<td>Maximum Output Voltage Swing</td>
<td>$R_L = 50k$</td>
<td>±12.8 ±13.4</td>
<td>±12.8 ±13.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 2k$</td>
<td>±12.0 ±12.8</td>
<td>±12.0 ±12.8</td>
<td>V</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** This parameter is tested on a sample basis only.

**Note 3:** Current noise is calculated from the formula:

\[ i_n = (2qI_B)^{1/2} \]

where \( q = 1.6 \times 10^{-19} \) coulomb. The noise of source resistors up to 1MΩ swamps the contribution of current noise.

**Note 4:** This parameter is not tested. It is guaranteed by design and by inference from the slew rate measurement.

**Note 5:** Overdrive recovery is defined as the time delay from the removal of an input overdrive to the output’s return from saturation to linear operation.

50% overdrive equals \( V_{IN} = \pm 2V \) (G = 10) or \( V_{IN} = \pm 200mV \) (G = 100).

**Note 6:** This parameter is not tested. It is guaranteed by design and by inference from other tests.

TYPICAL PERFORMANCE CHARACTERISTICS

**Small Signal Response, G = 10**
(Input = 50mV Pulse)

**Small Signal Response, G = 100**
(Input = 5mV Pulse)

**Slew Rate, G = 100**
(Input = ±130mV Pulse)

**Settling Time, G = 10**
(Input From –10V to 10V)

**Settling Time, G = 10**
(Input From 10V to –10V)

**Settling Time, G = 100**
(Input From –10V to 10V)

**Settling Time, G = 100**
(Input From 10V to –10V)
TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit Current vs Time

Gain Error vs Temperature

Gain Nonlinearity Over Temperature

Distribution of Offset Voltage

LT1102 • TPC17

LT1102 • TPC18

LT1102 • TPC19

LT1102 • TPC20
APPLICATIONS INFORMATION

In the two op amp instrumentation amplifier configuration, the first amplifier is basically in unity gain, and the second amplifier provides all the voltage gain. In the LT1102, the second amplifier is decompensated for gain of 10 stability, therefore high slew rate and bandwidth are achieved. Common mode rejection versus frequency is also optimized in the $G = 10$ mode, because the bandwidths of the two op amps are similar. When $G = 100$, this statement is no longer true; however, by connecting an 18pF capacitor between pins 1 and 2, a common mode AC gain is created to cancel the inherent roll-off. From 200Hz to 30kHz, CMRR versus frequency is improved by an order of magnitude.

Input Protection

Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1102 employs FET input transistors, consequently the differential input voltage can be ±30V (with ±15V supplies, ±36V with ±18V supplies). Some competitive instrumentation amplifiers have NPN inputs which are protected by back-to-back diodes. When the differential input voltage exceeds ±13V on these competitive devices, input current increases to milliampere level; more than ±10V differential voltage can cause permanent damage.

When the LT1102 inputs are pulled below the negative supply or above the positive supply, the inputs will clamp a diode voltage below or above the supplies. No damage will occur if the input current is limited to 20mA.

Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors ($= R_X$) between pins 1 and 2 and pins 7 and 8.

$$\text{Gain} = 10 + \frac{R_X}{R + R_X/90}$$

The nominal value of $R$ is 1.84kΩ. The usefulness of this method is limited by the fact that $R$ is not controlled to better than ±10% absolute accuracy in production. However, on any specific unit, 90R can be measured between Pins 1 and 2.
**Gain = 20, 110, or 200 Instrumentation Amplifiers**

**Differential Output**

**Single Ended Output**

Gain = 200, as shown
Gain = 20, short Pin 1 to Pin 2, Pin 7 to Pin 8 on both devices
Gain = 110, short Pin 1 to Pin 2, Pin 7 to Pin 8 on one device, not on the other
Input referred noise is reduced by \( \sqrt{2} \) (G = 200 or 20)

**Multiplexed Input Data Acquisition**

4 channels of differential input

800kHz signals can be multiplexed with LT1102 in G = 10

**Voltage Programmable Current Source is Simple and Precise**

**Dynamic Response of the Current Source**

A = 5V/DIV
B = 5mA/DIV
HORIZ. = 20µs/DIV
TYPICAL APPLICATIONS

Basic Connections

Settling Time Test Circuit

Offset Nulling

R1 = 910Ω, G = 10
R1 = 10k, G = 100
R2 = 3.3Ω, G = 10
R2 = 30Ω, G = 100
NULL RANGE = ±1mV
GAIN DEGRADATION = 0.018%

R1 = 910Ω, G = 10
R1 = 10k, G = 100
R2 = 3.3Ω, G = 10
R2 = 30Ω, G = 100
NULL RANGE = ±1mV
GAIN DEGRADATION = 0.018%
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

NOTE:
1. DIMENSIONS ARE INCHES
MILLIMETERS
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)
Ultra-Low Noise, Precision
OPERATIONAL AMPLIFIERS

FEATURES
- LOW NOISE: 4.5nV/√Hz max at 1kHz
- LOW OFFSET: 100µV max
- LOW DRIFT: 0.4µV/°C
- HIGH OPEN-LOOP GAIN: 117dB min
- HIGH COMMON-MODE REJECTION: 100dB min
- HIGH POWER-SUPPLY REJECTION: 94dB min
- FITS OP-07, OP-05, AD510, AND AD517 SOCKETS

APPLICATIONS
- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIERS
- RADIATION HARD EQUIPMENT

DESCRIPTION
The OPA27 and OPA37 are ultra-low noise, high-precision monolithic operational amplifiers.
Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.
A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full –40°C to +85°C temperature range.
The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.
The Texas Instruments’ OPA27 and OPA37 are improved replacements for the industry-standard OP-27 and OP-37.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.
ABSOLUTE MAXIMUM RATINGS(1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>±22V</td>
</tr>
<tr>
<td>Internal Power Dissipation (2)</td>
<td>500mW</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>±V_CC</td>
</tr>
<tr>
<td>Output Short-Circuit Duration (3)</td>
<td>Indefinite</td>
</tr>
<tr>
<td>Differential Input Voltage (4)</td>
<td>±0.7V</td>
</tr>
<tr>
<td>Differential Input Current (4)</td>
<td>±25mA</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>–55°C to +125°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>–40°C to +85°C</td>
</tr>
<tr>
<td>Lead Temperature:</td>
<td></td>
</tr>
<tr>
<td>P (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>U (soldering, 3s)</td>
<td>+260°C</td>
</tr>
</tbody>
</table>

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Maximum package power dissipation versus ambient temperature. (2) To common with ±V_CC = 15V. (4) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

[Diagram of pin configuration]

OFFSET TRIM

NC = No Connection
### ELECTRICAL CHARACTERISTICS

At $V_{CC} = \pm 15\, \text{V}$ and $T_A = +25^\circ\, \text{C}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>OPA27</th>
<th>OPA37</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT NOISE (^{(6)})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage, $f_0 = 10, \text{Hz}$</td>
<td></td>
<td></td>
<td></td>
<td>3.8</td>
<td>8.0</td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>$f_0 = 30, \text{Hz}$</td>
<td></td>
<td>3.3</td>
<td>5.6</td>
<td></td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>$f_0 = 1, \text{kHz}$</td>
<td></td>
<td>3.2</td>
<td>4.5</td>
<td></td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>$f_0 = 0.1, \text{Hz}$ to 10Hz</td>
<td></td>
<td>0.09</td>
<td>0.25</td>
<td></td>
<td></td>
<td></td>
<td>µV/√Hz</td>
</tr>
<tr>
<td>Current, (^{(1)} f_0 = 10, \text{Hz} )</td>
<td></td>
<td>1.7</td>
<td>1.7</td>
<td></td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
<tr>
<td>$f_0 = 30, \text{Hz}$</td>
<td></td>
<td>1.0</td>
<td>1.0</td>
<td></td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
<tr>
<td>$f_0 = 1, \text{kHz}$</td>
<td></td>
<td>0.4</td>
<td>0.6</td>
<td></td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
</tbody>
</table>

| OFFSET VOLTAGE \(^{(2)}\)        |                        |       |       |      |      |      |             |
| Input Offset Voltage             |                        |       |       |      |      |      |             |
| Average Drift \(^{(3)}\)         | $T_A_{MIN}$ to $T_A_{MAX}$ | ±25   | ±100  |      |      |      | µV         |
| Long Term Stability \(^{(4)}\)   |                        | ±0.4  | ±1.8  \(^{(6)}\) |      |      |      | µV/°C      |
| Supply Rejection                 | $V_{CC} = 4$ to 18V    | 94    | 120   |      |      |      | dB         |
|                                 | $V_{CC} = 4$ to 18V    | ±1    | ±20   |      |      |      | µV         |

| BIAS CURRENT                     |                        |       |       |      |      |      |             |
| Input Bias Current               |                        | ±15   | ±80   |      |      |      | nA         |

| OFFSET CURRENT                   |                        |       |       |      |      |      |             |
| Input Offset Current             |                        | 10    | 75    |      |      |      | nA         |

| IMPEDANCE                        |                        |       |       |      |      |      |             |
| Common-Mode                      |                        | 2 l 2.5 | GΩ l pF |

| VOLTAGE RANGE                    |                        |       |       |      |      |      |             |
| Common-Mode Input Range          |                        | ±11   | ±12.3 |      |      |      | V          |
| Common-Mode Rejection            | $V_{IN} = \pm 1\, \text{VDC}$ | 100   | 122   |      |      |      | dB         |

| OPEN-LOOP VOLTAGE GAIN, DC       |                        |       |       |      |      |      |             |
| $R_L = 2\, \text{kΩ}$            |                        | 117   | 124   |      |      |      | dB         |
| $R_L = 1\, \text{kΩ}$            |                        | 124   | 124   |      |      |      | dB         |

| FREQUENCY RESPONSE              |                        |       |       |      |      |      |             |
| Gain-Bandwidth Product \(^{(5)}\) | OPA27                  | 5 \(^{(6)}\) | 8    |      |      |      | MHz        |
|                                 | OPA37                  | 45 \(^{(6)}\) | 63   |      |      |      | MHz        |
| Slew Rate \(^{(5)}\)            | $V_{O} = \pm 10\, \text{V}$, $R_L = 2\, \text{kΩ}$ | OPA27, G = +1 | 1.7 \(^{(6)}\) | 1.9   |      |      | V/µs       |
|                                 |                        | OPA37, G = +5 | 11 \(^{(6)}\) | 11.9  |      |      | V/µs       |
|                                 | $R_L = 2\, \text{kΩ}$  | OPA27, G = +1 | 25   |      |      |      | µs         |
|                                 |                        | OPA37, G = +5 | 25   |      |      |      | µs         |

| RATED OUTPUT                    |                        |       |       |      |      |      |             |
| Voltage Output                  | $R_L = 2\, \text{kΩ}$  | ±12   | ±13.8 |      |      |      | V          |
|                                | $R_L = 600\, \text{Ω}$ | ±10   | ±12.8 |      |      |      | V          |
| Output Resistance               | DC, Open Loop          | 70    |      |      |      |      | Ω          |
| Short Circuit Current           | $R_L = 0\, \text{Ω}$  | 25    | 60 \(^{(1)}\) |      |      |      | mA         |

| POWER SUPPLY                    |                        |       |       |      |      |      |             |
| Rated Voltage                   |                        | ±15   |      |      |      |      | VDC        |
| Voltage Range,                   |                        |      |      |      |      |      |            |
| Derated Performance             |                        |      |      |      |      |      |            |
| Current, Quiescent              | $I_{O} = 0\, \text{mA}$ | ±4    | ±22   |      |      |      | VDC        |
|                                |                        | 3.3   | 5.7   |      |      |      | mA         |

| TEMPERATURE RANGE               |                        |       |       |      |      |      |             |
| Specification                   | $I_{O} = 0\, \text{mA}$ | −40   | +85   |      |      |      | °C         |
| Operating                       |                        | −40   | +85   |      |      |      | °C         |

**NOTES:** (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specification are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnullled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter specified by design.
## ELECTRICAL CHARACTERISTICS (Cont.)

At \( V_{CC} = \pm 15V \) and \(-40^\circ C \leq T_A \leq +85^\circ C\), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT VOLTAGE</strong>(^{(1)})</td>
<td>Input Offset Voltage</td>
<td>±48</td>
<td>±0.4</td>
<td>±220(^{(3)})</td>
<td>µV</td>
</tr>
<tr>
<td></td>
<td>Average Drift(^{(2)})</td>
<td>90(^{(3)})</td>
<td>122</td>
<td></td>
<td>µV/°C</td>
</tr>
<tr>
<td></td>
<td>Supply Rejection</td>
<td>±0.4</td>
<td>±1.8(^{(3)})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{CC} = 4.5 \text{ to } 18V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{CC} = 4.5 \text{ to } 18V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>BIAS CURRENT</strong></td>
<td>Input Bias Current</td>
<td>±21</td>
<td>±150(^{(3)})</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td><strong>OFFSET CURRENT</strong></td>
<td>Input Offset Current</td>
<td>20</td>
<td></td>
<td>135(^{(3)})</td>
<td>nA</td>
</tr>
<tr>
<td><strong>VOLTAGE RANGE</strong></td>
<td>Common-Mode Input Range</td>
<td>±10.5(^{(3)})</td>
<td>±11.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Common-Mode Rejection</td>
<td>96(^{(3)})</td>
<td>122</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>OPEN-LOOP GAIN, DC</strong></td>
<td>Open-Loop Voltage Gain</td>
<td>R(_L) = 2kΩ</td>
<td>113(^{(3)})</td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td><strong>RATED OUTPUT</strong></td>
<td>Voltage Output</td>
<td>R(_L) = 2kΩ</td>
<td>±11.0(^{(3)})</td>
<td>±13.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Short Circuit Current</td>
<td>V(_O) = 0VDC</td>
<td>25</td>
<td></td>
<td>mA</td>
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<tr>
<td><strong>TEMPERATURE RANGE</strong></td>
<td>Specification</td>
<td>-40</td>
<td></td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Offset voltage specification are measured with automatic test equipment after approximately 0.5s from power turn-on.
2. Unnulled or nulled with 8kΩ to 20kΩ potentiometer.
3. This parameter specified by design.

---

**Texas Instruments**

www.ti.com

OPA27, OPA37

SBOS135C
TYPICAL CHARACTERISTICS

At $T_a = +25^\circ C$, $\pm V_{CC} = \pm 15VDC$, unless otherwise noted.

INFORMATION OCTOBER 2020

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This industry-standard equation is inaccurate and these figures should be used for comparison purposes only!

Warning: This industry-standard equation is inaccurate and these figures should be used for comparison purposes only!
TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ C$, $\pm V_{CC} = \pm 15VDC$, unless otherwise noted.

**Input Voltage Noise Spectral Density**

**Open-Loop Frequency Response**

**Bias and Offset Current vs Temperature**

**OPA27 Closed-Loop Voltage Gain and Phase Shift vs Frequency ($G = 100$)**

**OPA37 Closed-Loop Voltage Gain and Phase Shift vs Frequency ($G = 100$)**

**Common-Mode Rejection vs Frequency**
TYPICAL CHARACTERISTICS (Cont.)

At \( T_A = +25^\circ C, \pm V_{CC} = \pm 15VDC \), unless otherwise noted.

![Graphs showing various electrical characteristics of OPA27 and OPA37 amplifiers.]
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ C$, $\pm V_{CC} = \pm 15VDC$, unless otherwise noted.

**OPA37 SMALL SIGNAL TRANSIENT RESPONSE**

- Output Voltage (mV) vs. Time (µs)
- $A_V = +5$
- $C_L = 25pF$

**OPA27 LARGE SIGNAL TRANSIENT RESPONSE**

- Output Voltage (V) vs. Time (µs)
- $A_{VCL} = +1$

**OPA37 LARGE SIGNAL TRANSIENT RESPONSE**

- Output Voltage (V) vs. Time (µs)
- $A_V = +5$
APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA27 and OPA37 offset voltages are laser-trimmed and require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used, but $V_{OS}$ drift will be degraded by an additional $0.1\mu V/°C$ to $0.2\mu V/°C$. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately $3.3\mu V/°C$ per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27 and OPA37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

THERMEOLECTRIC POTENTIALS

The OPA27 and OPA37 are laser-trimmed to microvolt-level input offset voltages, and for very-low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMFs if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference (see Figure 11).

Short, direct mounting of the OPA27 and OPA37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

**NOTE:** All capacitor values are for nonpolarized capacitors only.

FIGURE 2. Low Frequency Noise.

0.1Hz TO 10Hz NOISE

1s/div  40mv/div
**NOISE: BIPOLAR VERSUS FET**

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ, the OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27, as shown in Figure 5.

**COMPENSATION**

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_F) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_F and C_IN and eliminate peaking or oscillation.

**INPUT PROTECTION**

Back-to-back diodes are used for input protection on the OPA27 and OPA37. Exceeding a few hundred millivolts differential input signal will cause current to flow, and without external current limiting resistors, the input will be destroyed. Accidental static discharge, as well as high current, can damage the amplifier’s input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged, as will any precision operational amplifier subjected to this abuse.

Transient conditions can cause feedthrough due to the amplifier’s finite slew rate. When using the OPA27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended, as shown in Figure 6.

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FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

FIGURE 10. NAB Tape Head Preamplifier.

FIGURE 11. Low Frequency Noise Comparison.

A. 741 noise with circuit well-shielded from air currents and RFI. (Note scale change.)

B. OP-07AH with circuit well-shielded from air currents and RFI.

C. OPA27AJ with circuit well-shielded from air currents and RFI. (Represents ultimate OPA27 performance potential.)

D. OPA27 with circuit unshielded and exposed to normal lab bench-top air currents. (External thermoelectric potentials far exceed OPA27 noise.)

E. OPA27 with heat sink and shield which protects input leads from air currents. Conditions same as (D).
FIGURE 12. Low Noise Instrumentation Amplifier.

FIGURE 13. Hydrophone Preamplifier.


FIGURE 15. High Performance Synchronous Demodulator.
Gain = -1010 V/V
$V_{OS} = 2$ mV
Drift = 0.07 μV/°C
$e_n = 1$ nV/√Hz at 10 Hz
0.9 nV/√Hz at 100 Hz
0.87 nV/√Hz at 1 kHz
Full Power Bandwidth = 180 kHz
Gain Bandwidth = 500 MHz
Equivalent Noise Resistance ≈ 50 Ω

Signal-to-Noise Ratio = $\sqrt{N}$
since amplifier noise is uncorrelated.

N = 10 Each OPA37

FIGURE 17. Unity-Gain Buffer.

FIGURE 18. High Slew Rate Unity-Gain Buffer.

FIGURE 19. RF Detector and Video Amplifier.


\[ f_{\text{OUT}} = \text{RPM} \cdot N \]

Where \( N \) = Number of Gear Teeth
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
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<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4)</th>
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<td>OPA37U</td>
<td>Samples</td>
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</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green:** TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
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**TAPE AND REEL INFORMATION**

### TAPE DIMENSIONS

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<td>Dimension designed to accommodate the component length</td>
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<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
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<td>Overall width of the carrier tape</td>
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<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
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### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal*

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*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.

4. This dimension does not include interlead flash.

5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
P (R-PDIP-T8)  PLASTIC DUAL-IN-LINE PACKAGE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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