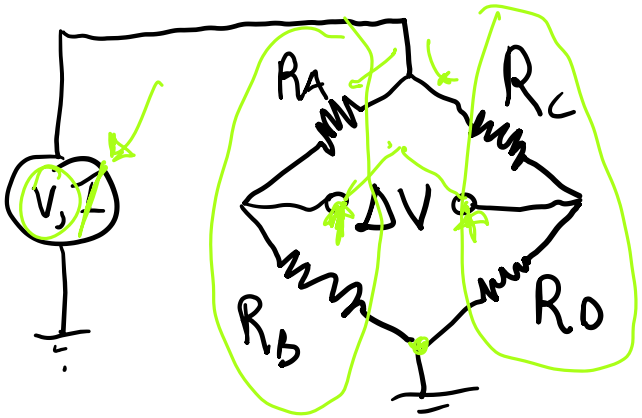
Instrumentation amplifiers, load-cell amplification, a review of the experiment, current measurement and some current sources

Week 7: AoE 7.09-7.12; 15.03

Keithley low-level measurements handbook

The Wheatstone bridge



Suppose we have a constant *V* bridge excitation. Then the total current passing through the bridge is:

$$I_{tot} = \frac{V}{(R_A + R_B)||(R_C + R_D)}$$

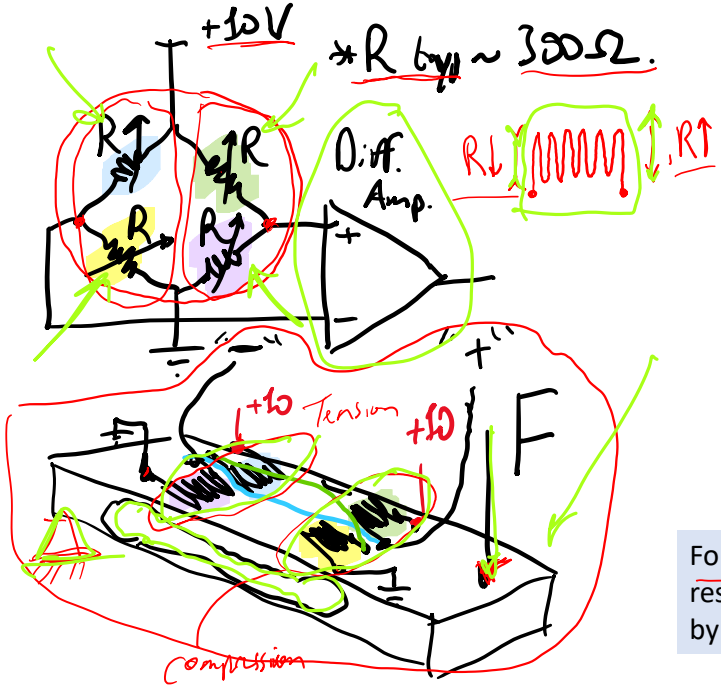
For simplicity, and to get an idea of how this bridge works, let's assume that both dividers have an equal resistance, and furthermore that all resister values are identical. Then $\Delta V = 0$.

Now, consider a case where R_A increases by an amound dR, and R_D decreases by dR.
In this case, the current passing through the two halves of the bridge (each a divider!) is no longer identical. In fact, the left current is: $V/(R_A + dR + R_B)$, while the right current is $V/(R_C + R_D - dR)$.

Thus, the voltage on the left is $R_B * V / (R_A + dR + R_B)$, and on the right, $(R_D - dR)*V/(R_C + R_D - dR)$, and after a significant amount of algebra, we find to leading order that $\Delta V \sim 2\ dR$ (the exact calculation you can do if you like!)

Fundamentally, this circuit becomes ***non-linear*** when dR becomes large compared with all the R in the bridge.

A load-cell circuit consisting of strain gages in the Wheatstone-bridge configuration:



Upon application of force, F, the strain gauges respond by changing their resistance. Under *compression,* the resistance *decreases;* under *tension,* the resistance *increases.*

Thus we can quickly see that the differential voltage will systematically change in response to applied force, as the v-dividers formed by the strain gauges in each side of the load cell will change their primary voltage values in a levered-fashion.

Nevertheless, the mean value sits around **5 V!**

– There is intrinsically a high common-mode voltage.

For discussion on Piazza: why would one wish to ensure that the resistors in each leg see the same amount of current, as is achieved by this bridge configuration?

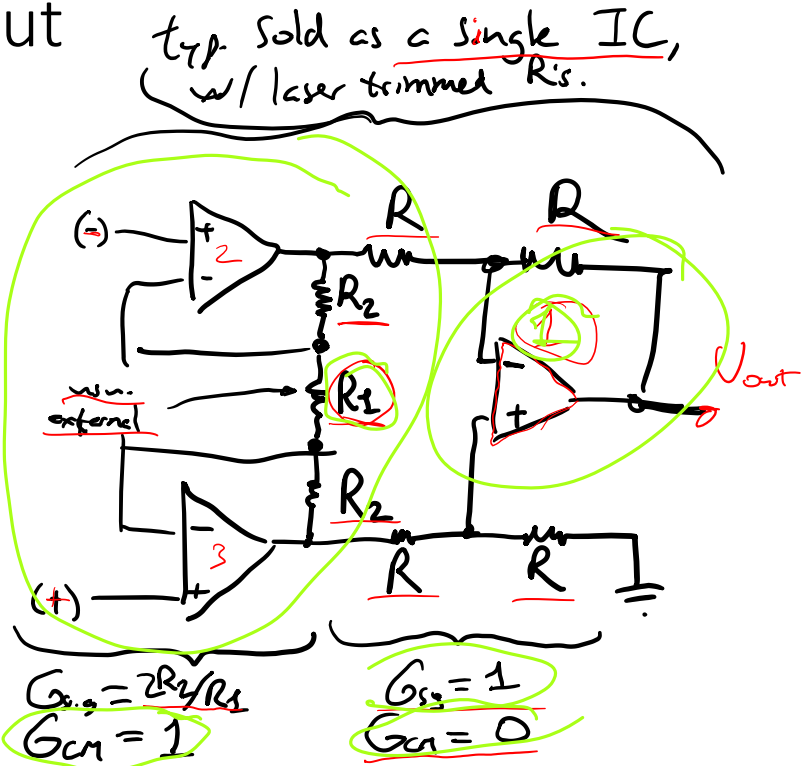
Often we are tasked with the measurement of a transducer's output

The main challenge addressed by instrumentation amplifiers is *high rejection of common-mode voltage (CMRR)*

The high CMRR is necessary because often transducers (such as load cells) have high common-mode signals (of order several V), while the signal of interest is a differential signal in the mV-scale.

If we want a 0.1% accuracy of a mV signal, say, then we must reject 5 V-common-mode down to the microvolt level (!) this corresponds to a rejection of over a million times the common-mode!

How can we achieve this?

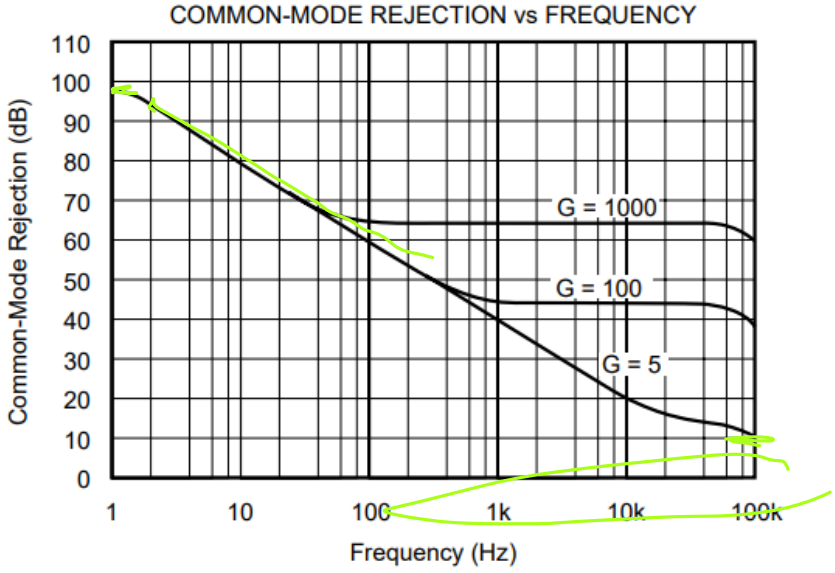


The previous circuit should look familiar from the handout on instrumentation amplifiers.

These are useful devices for discarding common-mode signals!

A word of caution on CMRR in INAs: see from the INA 122 datasheet:

CMRR drops at high-frequency!



2-wire vs. 4-wire measurement of low-R

FIGURE 3-14: Two-Wire Resistance Measurement

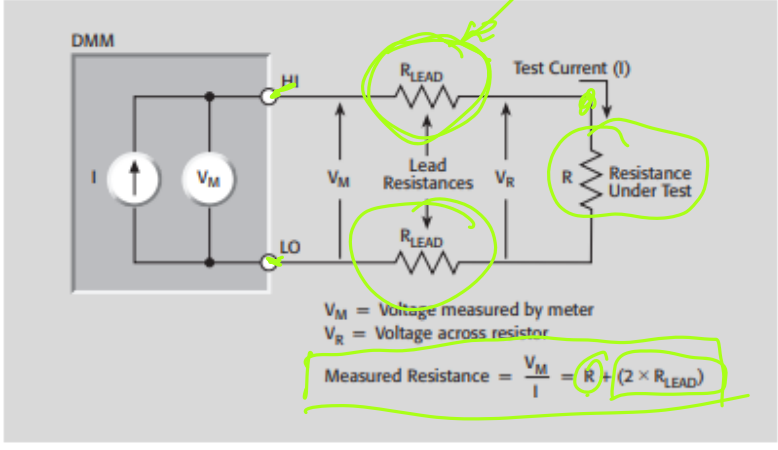
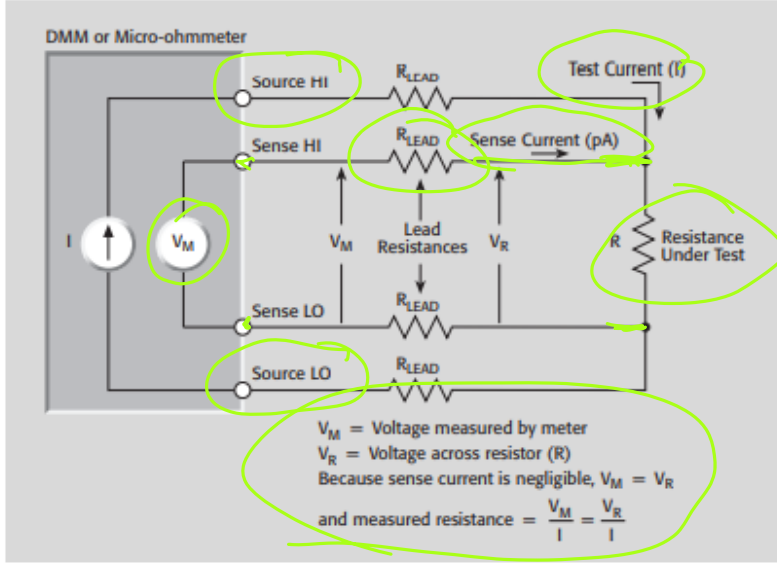


FIGURE 3-15: Four-Wire Resistance Measurement



The bulk resistivity of aluminum is ~ 2.8 e -8 Ohm.meters. The coating thickness is ca. 30 nm, the sample is 5 cm wide, and the gage between conductors is ca. 5 cm. You can thus estimate R_{alu}; if it is less than 100 Ohm, 4 wire is needed!

Keithley low-level meas. Handbk.

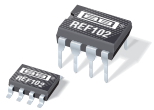
Exercises this week:

1. Measure the resistance of an uncracked sample -> 4-wire method. Use copper strips to ensure you're measuring across the whole coating.
2. Measure the `cracked' sample to get an idea of the range of R you should expect.
3. Design your Wheatstone bridge, specifying the values of R in the other legs. Build a voltage source for the bridge (bridge `excitation'). Keep in mind the power dissipated by the bridge!
4. Come up with a way to measure crack length and velocity based on the resistance of the plate and your bridge architecture. Can you do both? How? I'll briefly introduce some helpful amplifiers / circuits now.

Voltage sources & current sources: REF 102

A new arrival: high-GBP instrumentation amp, LT1102

A fast, non-unity gain-stable op-amp: OPA 37



SBVS022B – SEPTEMBER 2000 – REVISED JUNE 2009

10V Precision Voltage Reference

FEATURES

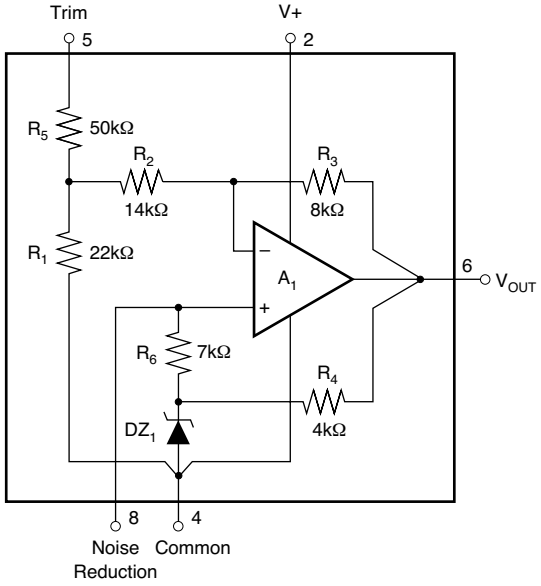
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μV_{PP} typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: PLASTIC DIP, SO-8

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETER
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max C-grade over the industrial temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single-supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.



ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage	+40V
Operating Temperature	
P, U	–25°C to +85°C
Storage Temperature Range	
P, U	–40°C to +125°C
Short-Circuit Protection to Common or V+	Continuous

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

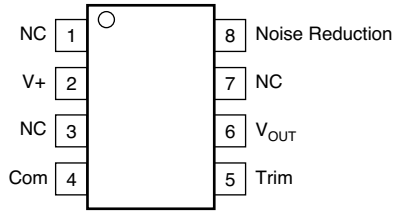
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAX INITIAL ERROR (mV)	MAX DRIFT (PPM/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
REF102AU	±10	±10	SO-8	D	REF102AU
REF102AP	±10	±10	DIP-8	P	REF102AP
REF102BU	±5	±5	SO-8	D	REF102BU
REF102BP	±5	±5	DIP-8	P	REF102BP
REF102CU	±2.5	±2.5	SO-8	D	REF102CU
REF102CP	±2.5	±2.5	DIP-8	P	REF102CP

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

PIN CONFIGURATIONS

Top View **DIP, SO**



NC = Not Connected

ELECTRICAL CHARACTERISTICS

At T_A = +25°C and V_S = +15V power supply, unless otherwise noted.

PARAMETER	CONDITIONS	REF102A			REF102B			REF102C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE											
Initial	T_A = 25°C	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature (1)				10			5			2.5	ppm/°C
vs Supply											
(Line Regulation)	V_S = 11.4V to 36V			2			1			1	ppm/V
vs Output Current											
(Load Regulation)	I_L = 0mA to +10mA			20			10			10	ppm/mA
	I_L = 0mA to –5mA			40			20			20	ppm/mA
vs Time	T_A = +25°C										
M Package			5			✻			✻		ppm/1000hr
P, U Packages (2)			20			✻					ppm/1000hr
Trim Range (3)		±3			✻			✻			%
Capacitive Load, max			1000			✻			✻		pF
NOISE	0.1Hz to 10Hz		5			✻			✻		μV_{PP}
OUTPUT CURRENT		+10, –5			✻			✻			mA
INPUT VOLTAGE RANGE		+11.4		+36	✻		✻	✻		✻	V
QUIESCENT CURRENT	I_{OUT} = 0			+1.4			✻			✻	mA
WARM-UP TIME (4)	To 0.1%		15			✻			✻		µs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		–25		+85	✻		✻	✻		✻	°C

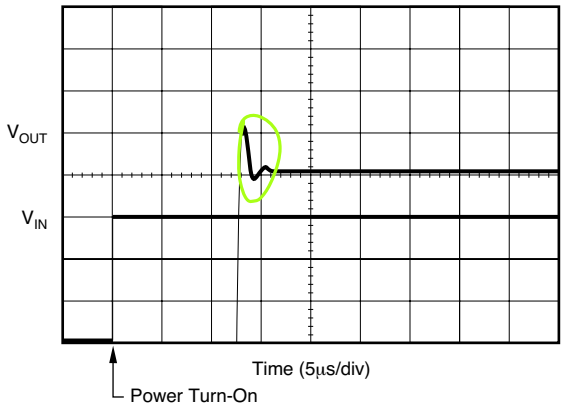
✻ Specifications same as REF102A.

NOTES: (1) The *box* method is used to specify output voltage drift vs temperature; see the Discussion of Performance section.
(2) Typically 5ppm/1000hrs after 168hr powered stabilization.
(3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details.
(4) With noise reduction pin floating. See Typical Characteristics for details.

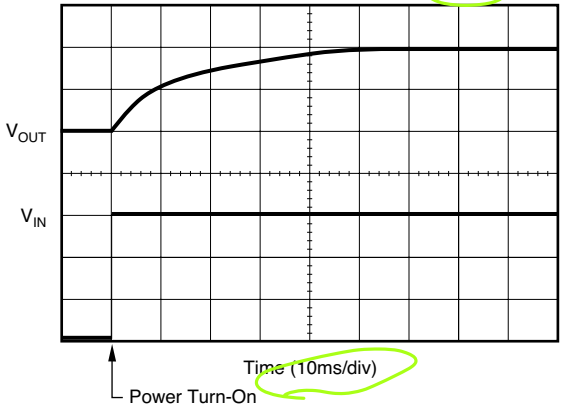
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +15V, unless otherwise noted.

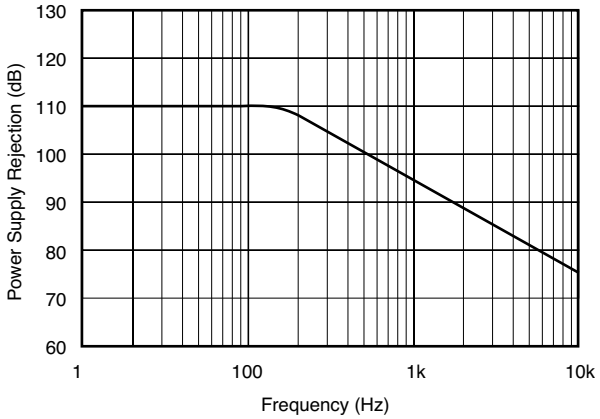
POWER TURN-ON RESPONSE



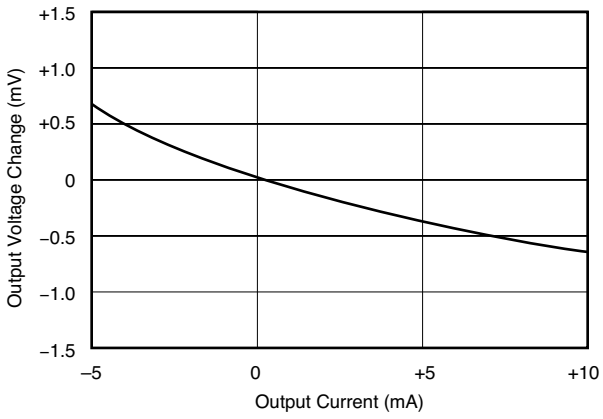
POWER TURN-ON RESPONSE with 1µF C_N



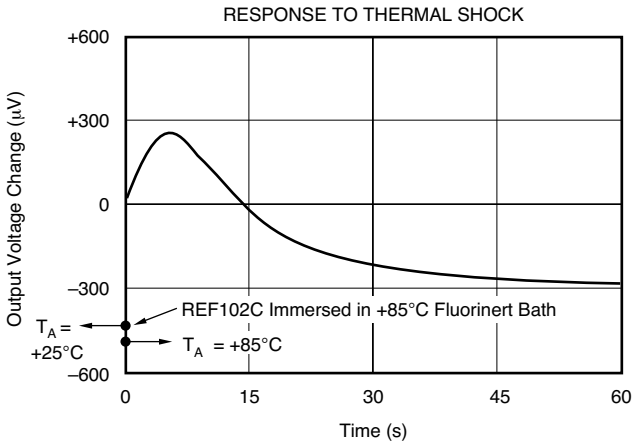
POWER SUPPLY REJECTION vs FREQUENCY



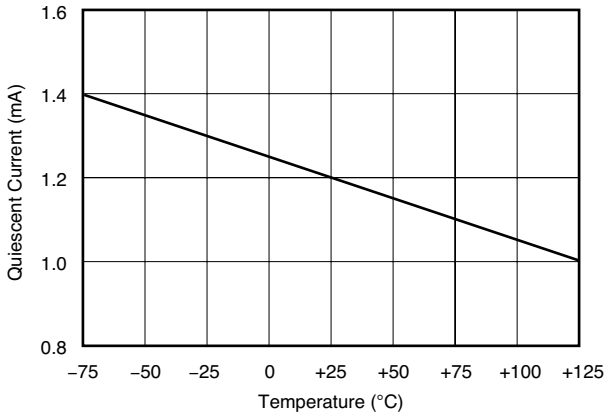
LOAD REGULATION



RESPONSE TO THERMAL SHOCK



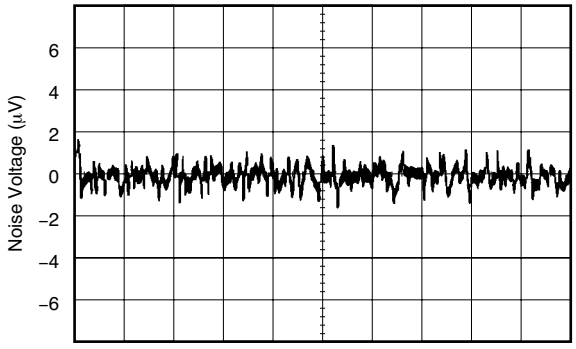
QUIESCENT CURRENT vs TEMPERATURE



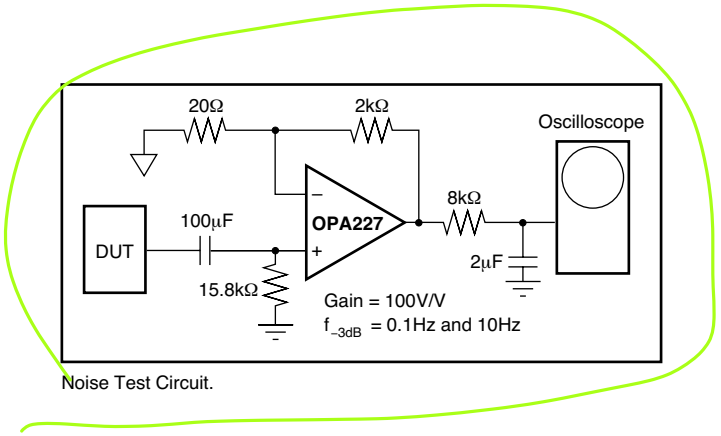
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +15V, unless otherwise noted.

TYPICAL REF102 REFERENCE NOISE



Low Frequency Noise (1s/div)
(See Noise Test Circuit)



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1, op amp A_1, and resistor network $R_1 – R_6$.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1. R_1, R_2, and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4. R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the temperature coefficient (TCR) of of R_5 closely matches the TCR of R_1, R_2 and R_3 , the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the *butterfly method* and the *box method*. The REF102 is specified by the more commonly-used *box method.* The *box* is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not known, either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CU as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The *box* height, V_1 to V_2, is 2.75mV.

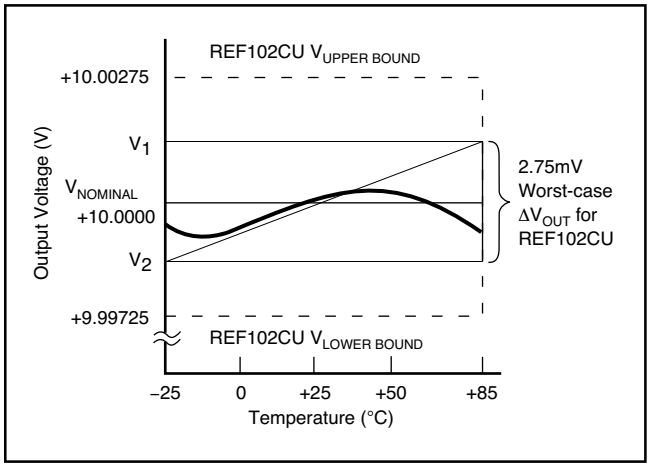
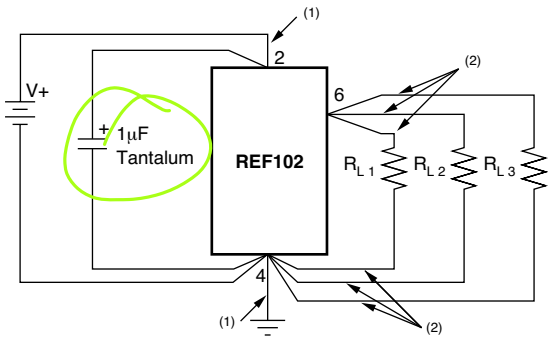


FIGURE 1. REF102CU Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated, being sure to minimize interconnection resistances.



NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

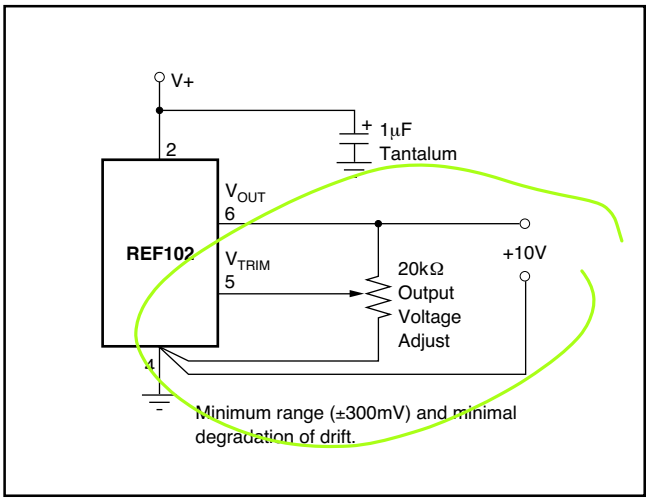


FIGURE 3. REF102 Optional Output Voltage Adjust.

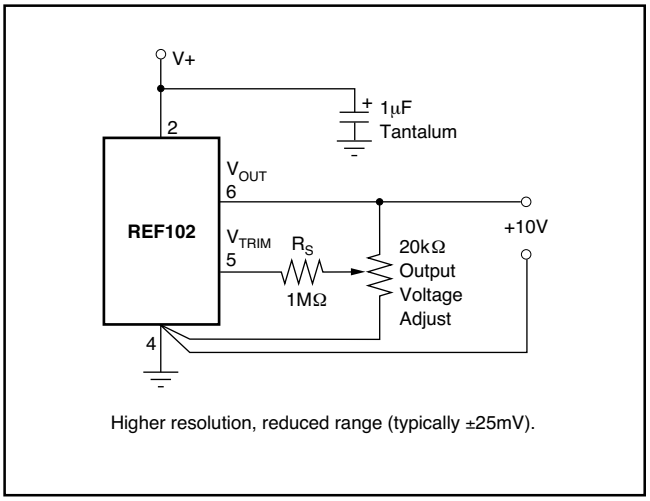


FIGURE 4. REF102 Optional Output Voltage, Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low-pass filter with R_6 (refer to the figure on page 1) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1μF noise reduction capacitor on the high-frequency noise of the REF102. R_6 is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about $800\mu V_{PP}$ to under $200\mu V_{PP}$. If further noise reduction is required, use the circuit in Figure 14.

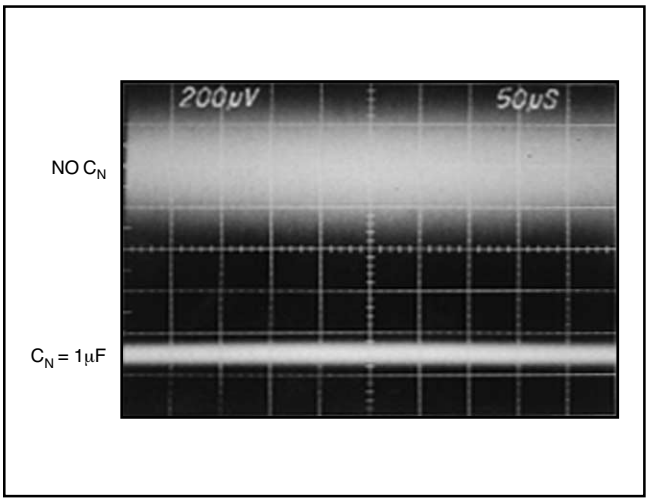


FIGURE 5. Effect of 1μF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz)

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

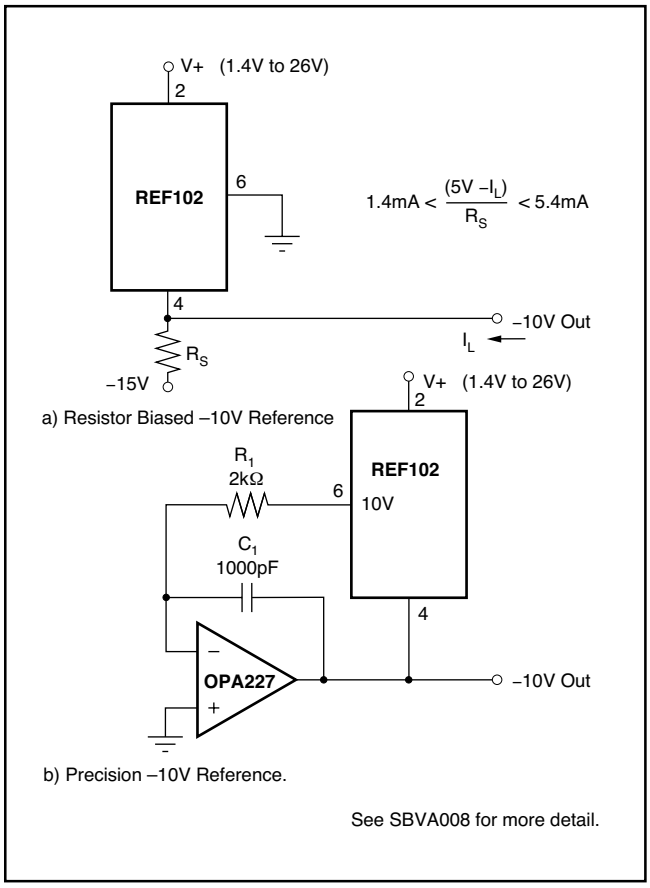


FIGURE 6. –10V Reference Using a) Resistor or b) OPA227.

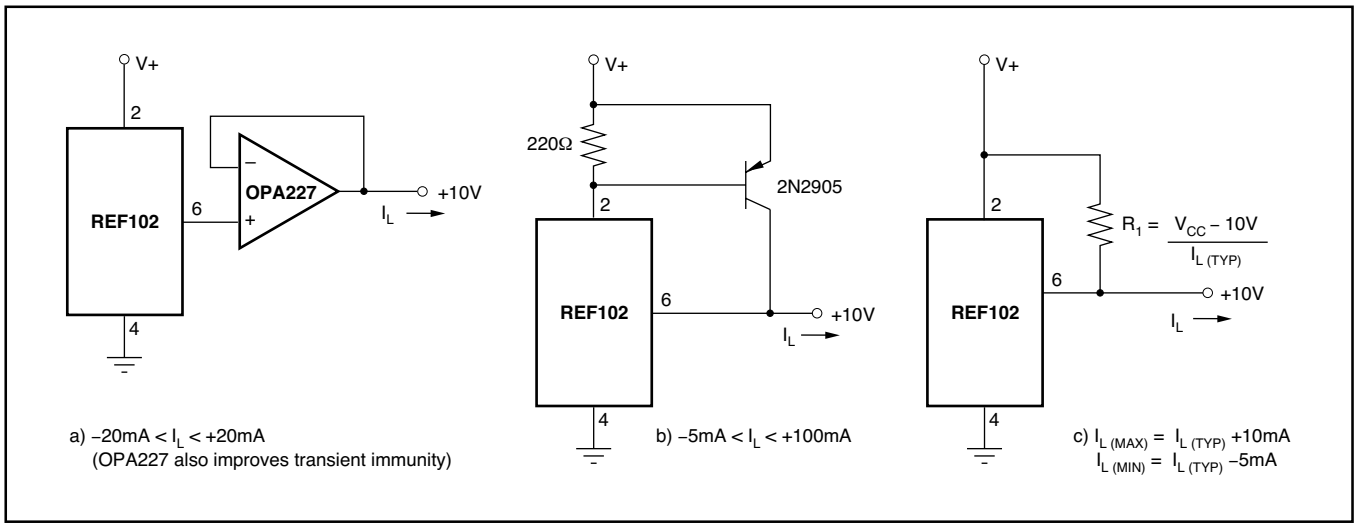


FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L\,(TYP)}$ +10mA, –5A.

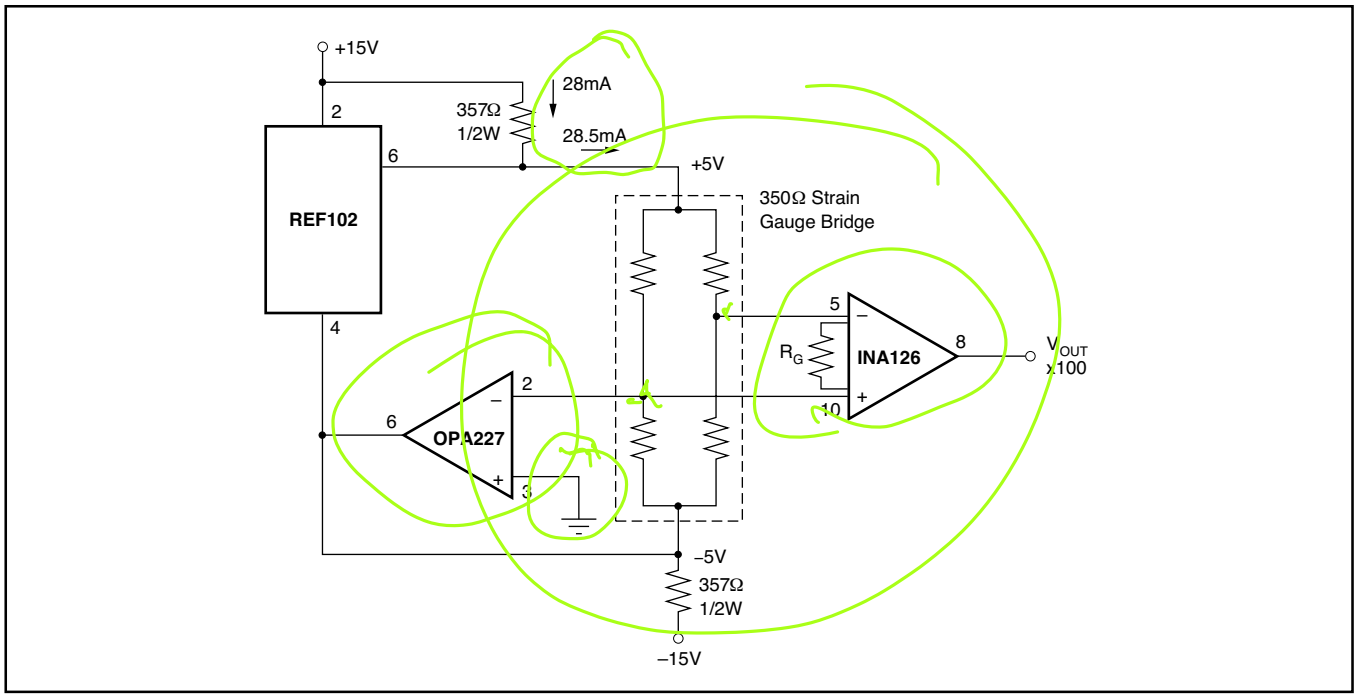


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

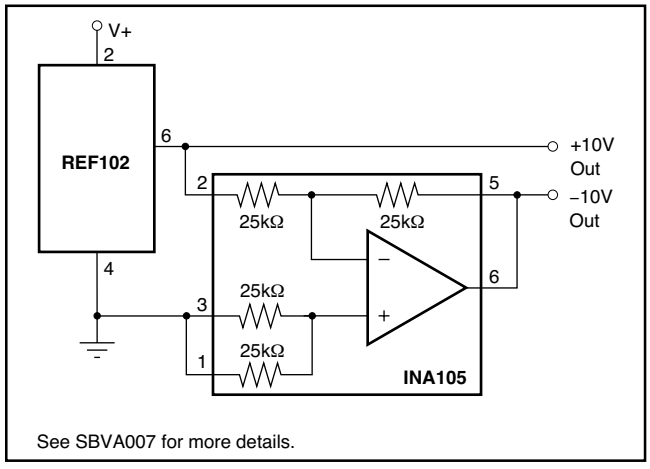


FIGURE 9. ±10V Reference.

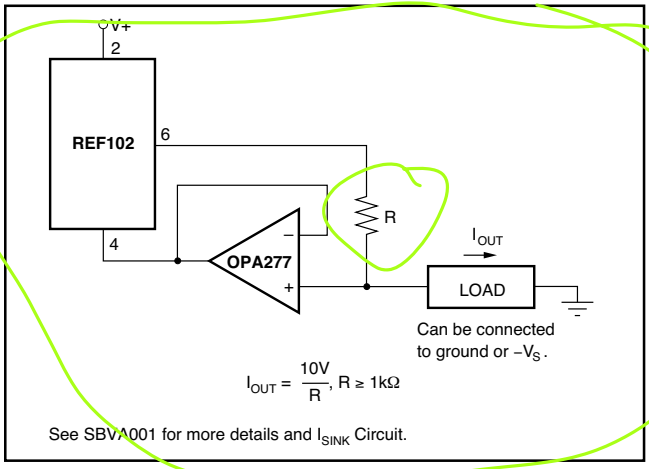
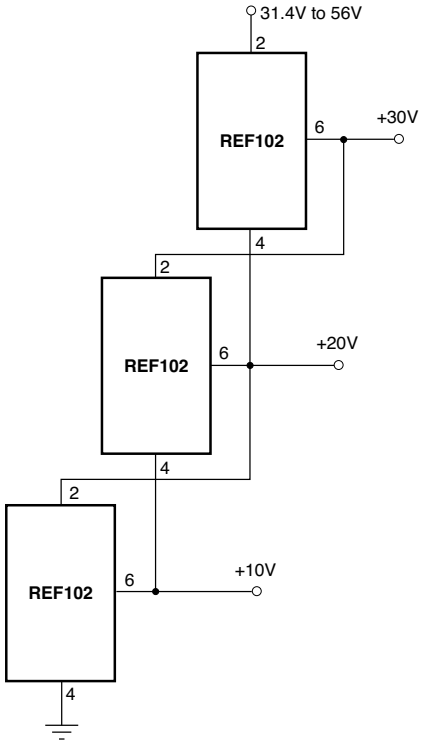


FIGURE 10. Positive Precision Current Source.



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26, where *n* is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

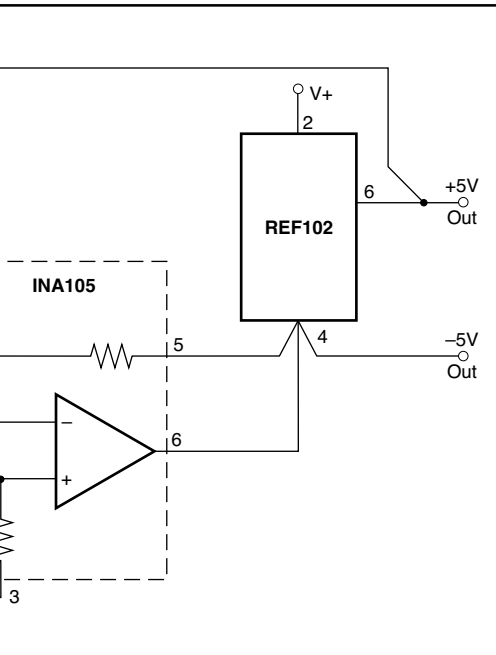


FIGURE 12. ±5V Reference.

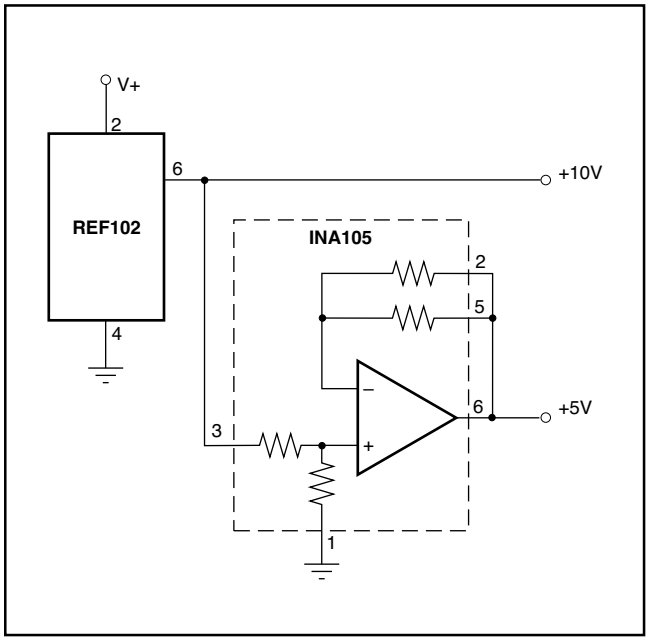


FIGURE 13. +5V and +10V Reference.

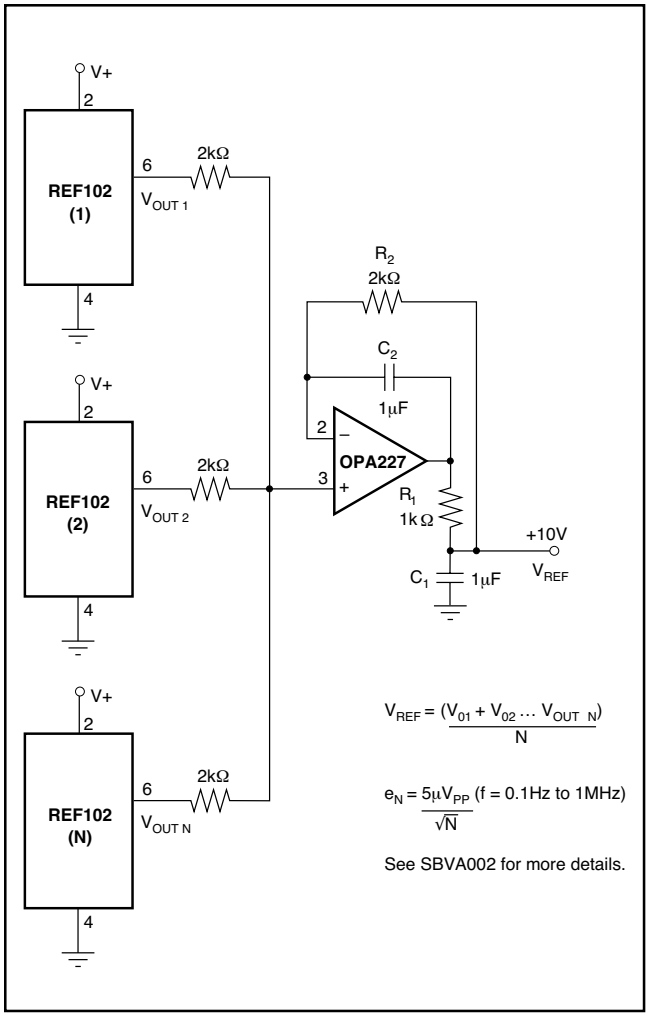


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
6/09	B	2	Absolute Maximum Ratings	Deleted lead temperature rating.
			Package/Ordering Information	Changed Package Ordering Information table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF102AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		REF102P A	Samples
REF102AU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102AU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102AUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		REF 102U A	Samples
REF102BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		REF102P B	Samples
REF102BU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U B	Samples
REF102BUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U B	Samples
REF102CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	REF102P C	Samples
REF102CPG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	REF102P C	Samples
REF102CU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples
REF102CU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples
REF102CUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	REF 102U C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

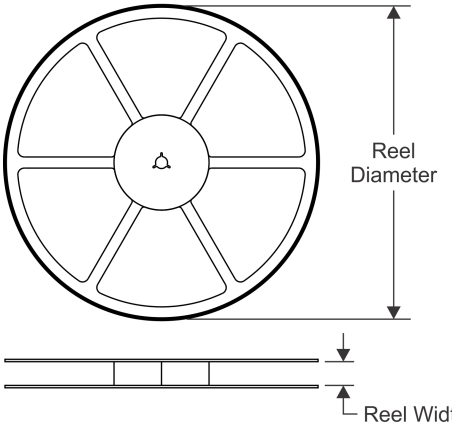
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

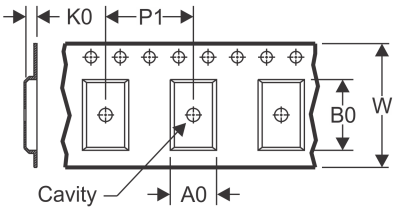
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

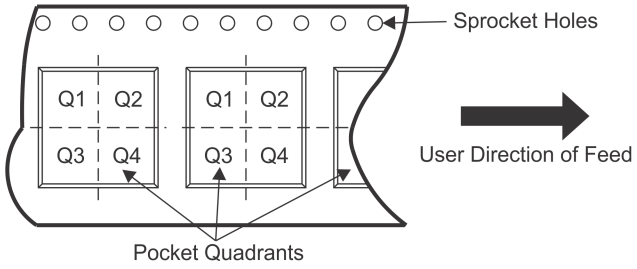


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

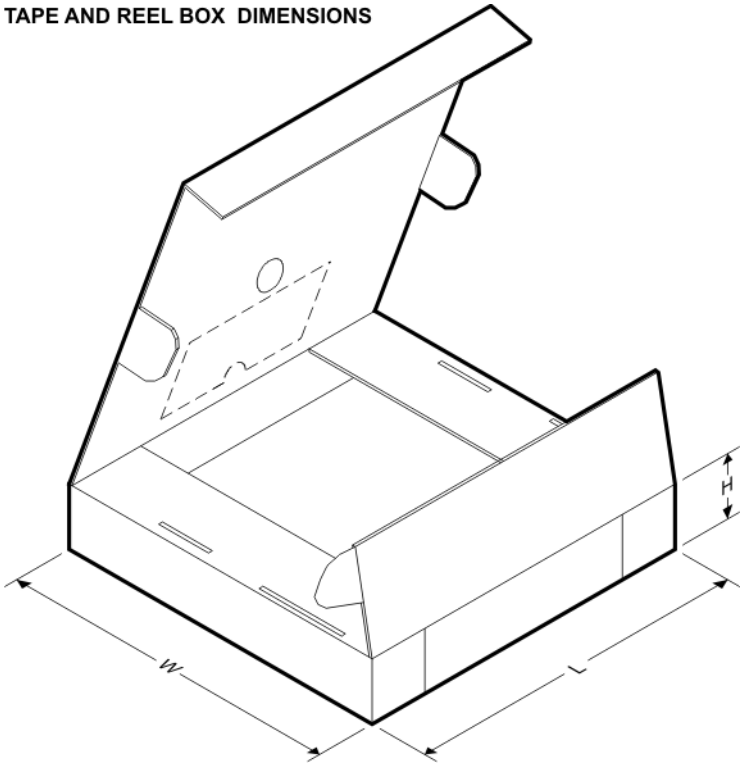
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF102AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF102CU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

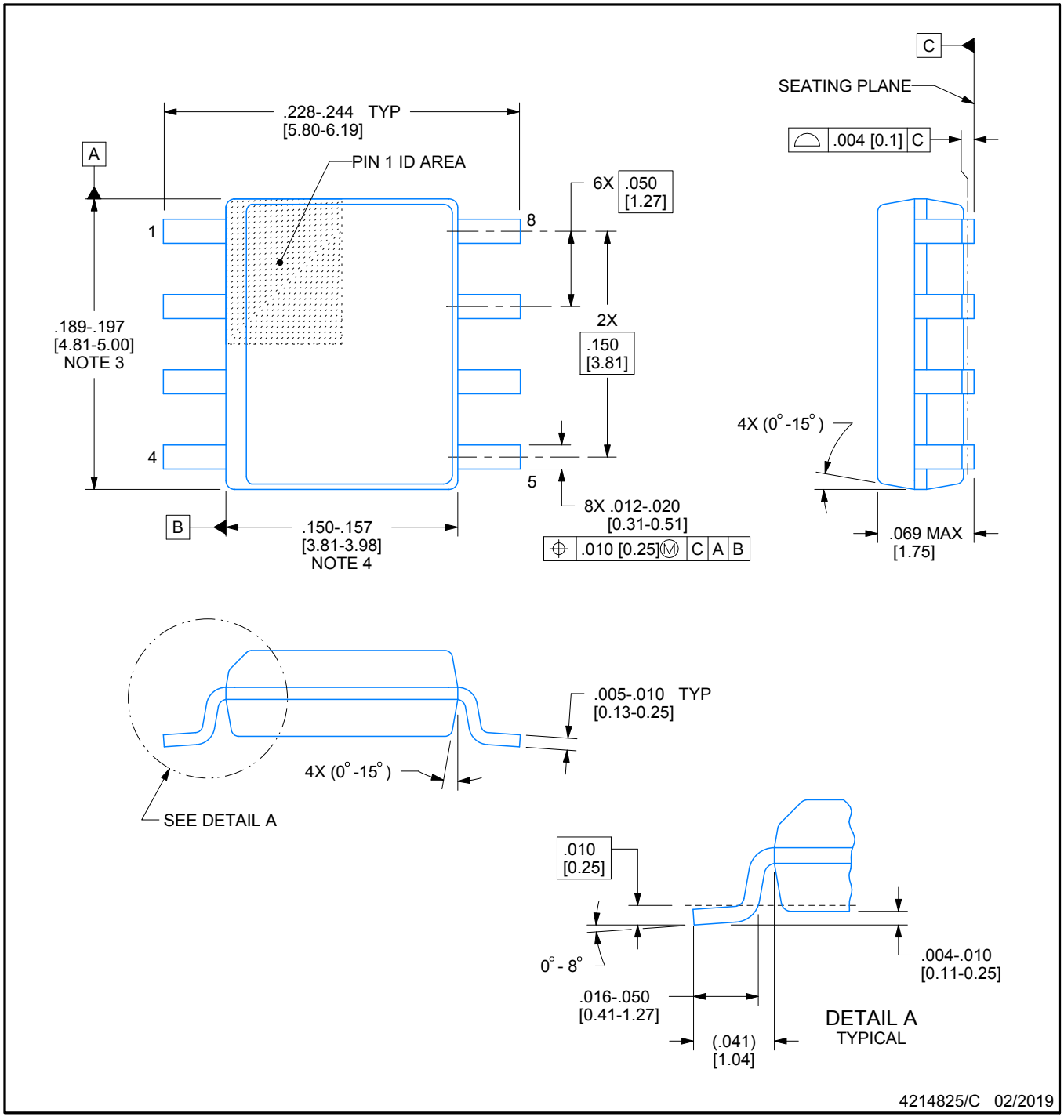
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF102AU/2K5	SOIC	D	8	2500	853.0	449.0	35.0
REF102CU/2K5	SOIC	D	8	2500	853.0	449.0	35.0

PACKAGE OUTLINE

D0008A

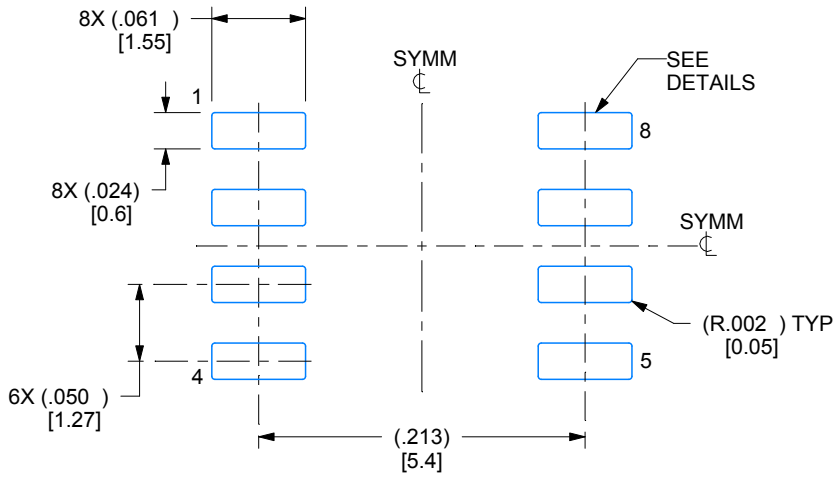
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

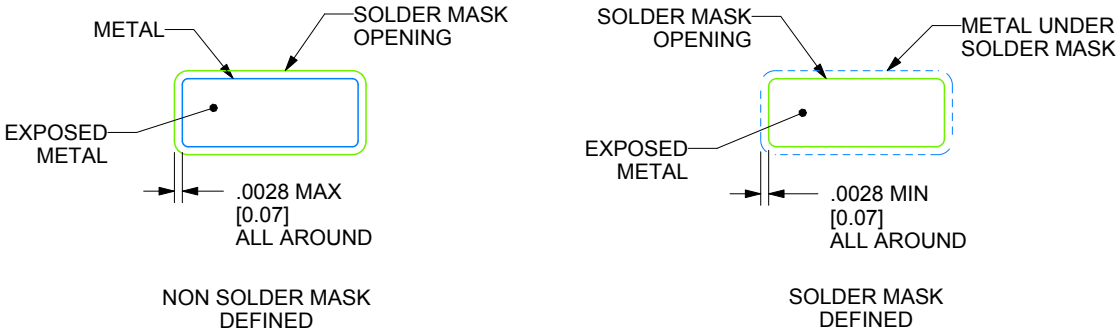


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

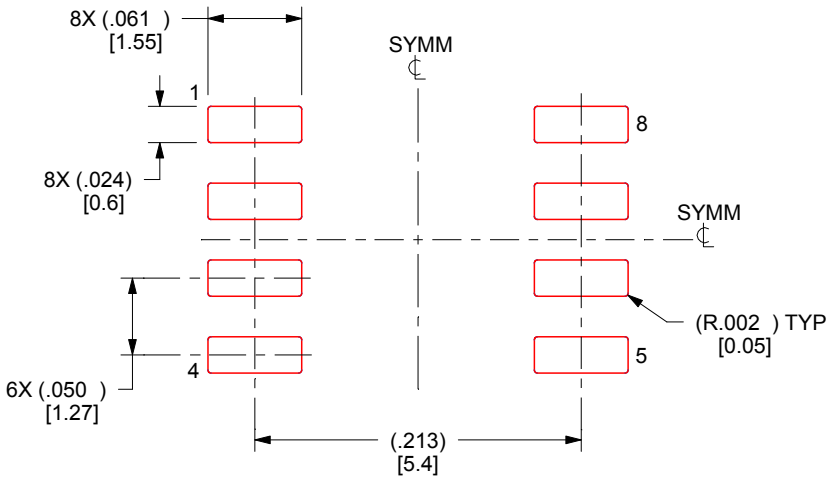


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



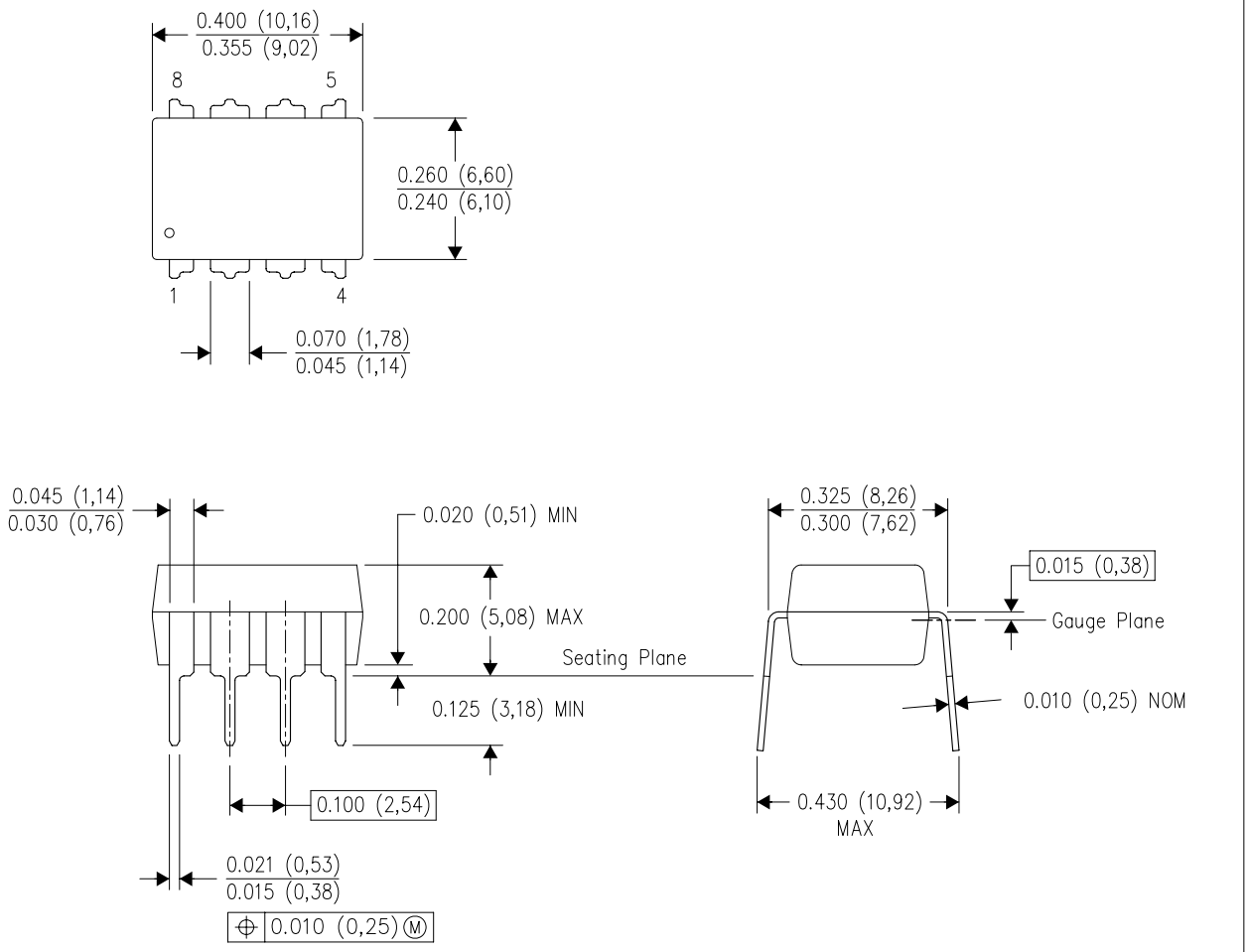
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)

FEATURES

- Slew Rate: 30V/µs
- Gain-Bandwidth Product: 35MHz
- Settling Time (0.01%): 3µs
- Overdrive Recovery: 0.4µs
- Gain Error: 0.05% Max
- Gain Drift: 5ppm/°C
- Gain Nonlinearity: 16ppm Max
- Offset Voltage (Input + Output): 600µV Max
  – Drift with Temperature: 2µV/°C
- Input Bias Current: 40pA Max
- Input Offset Current: 40pA Max
  – Drift with Temperature (to 70°C): 0.5pA/°C

APPLICATIONS

- Fast Settling Analog Signal Processing
- Multiplexed Input Data Acquisition Systems
- High Source Impedance Signal Amplification from High Resistance Bridges, Capacitance Sensors, Photodetector Sensors
- Bridge Amplifier with < 1Hz Lowpass Filtering

DESCRIPTION

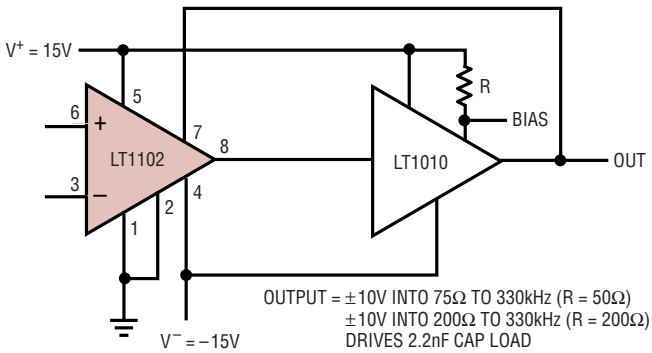
The LT®1102 is the first fast FET input instrumentation amplifier offered in the low cost, space saving 8-pin packages. Fixed gains of 10 and 100 are provided with excellent gain accuracy (0.01%) and non-linearity (3ppm). No external gain setting resistor is required.

Slew rate, settling time, gain-bandwidth product, overdrive recovery time are all improved compared to competitive high speed instrumentation amplifiers.

Industry best speed performance is combined with impressive precision specifications: less than 10pA input bias and offset currents, 180µV offset voltage. Unlike other FET input instrumentation amplifiers, on the LT1102 there is no output offset voltage contribution to total error, and input bias currents do not double with every 10°C rise in temperature. Indeed, at 70°C ambient temperature the input bias current is only 40pA.

TYPICAL APPLICATION

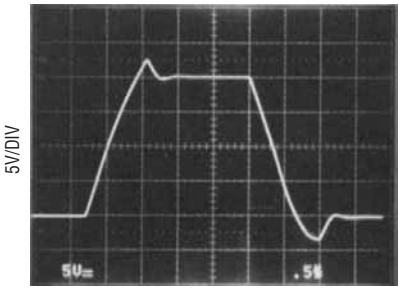
Wideband Instrumentation Amplifier with ±150mA Output Current



OUTPUT = ±10V INTO 75Ω TO 330kHz (R = 50Ω)
±10V INTO 200Ω TO 330kHz (R = 200Ω)
DRIVES 2.2nF CAP LOAD
GAIN = 10, DEGRADED 0.01% DUE TO LT1010

LT1102 • TA01

Slew Rate



G = 10 0.5µs/DIV LT1102 • TA02

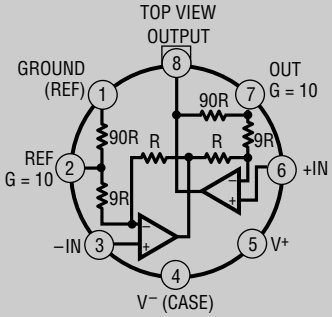
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±40V
Input Voltage ..... ±20V

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
LT1102I ..... –40°C to 85°C
LT1102AC/LT1102C ..... 0°C to 70°C
LT1102AM/LT1102M **(OBSOLETE)**.....–55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

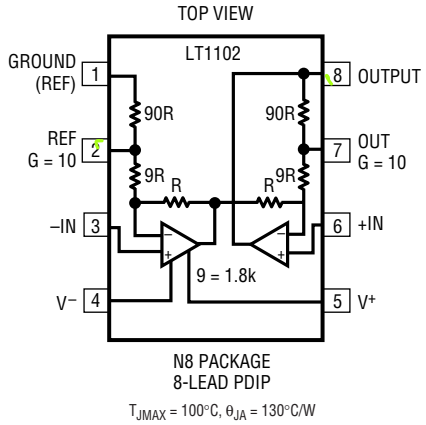


H PACKAGE
8-LEAD TO-5 METAL CAN

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

ORDER PART NUMBER

LT1102AMH
LT1102MH
LT1102ACH
LT1102CH



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 100°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1102IN8
LT1102ACN8
LT1102CN8

J8 PACKAGE
8-LEAD CERDIP

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

LT1102MJ8
LT1102CJ8

LT1102 • POI01

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, Gain = 10 or 100, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM/AC MIN	LT1102AM/AC TYP	LT1102AM/AC MAX	LT1102M/I/C MIN	LT1102M/I/C TYP	LT1102M/I/C MAX	UNITS
G_E	Gain Error	V_O = ±10V, R_L = 50k or 2k		0.010	0.050		0.012	0.070	%
G_{NL}	Gain Nonlinearity	G = 100, R_L = 50k G = 100, R_L = 2k G = 10, RL = 50k or 2k		3 8 7	14 20 16		4 8 7	18 25 30	ppm ppm ppm
V_{OS}	Input Offset Voltage			180	600		200	900	µV
I_{OS}	Input Offset Current			3	40		4	60	pA
I_B	Input Bias Current			±3	±40		±4	±60	pA
	Input Resistance Common Mode Differential Mode	 V_{CM} = –11V to 8V V_{CM} = 8V to 11V 		 10^{12} 10^{11} 10^{12}			 10^{12} 10^{11} 10^{12}		 Ω Ω Ω
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.8			2.8		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz f_O = 1000Hz (Note 2)		37 19	 30		37 20		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Input Noise Current Density	f_O = 1000Hz, 10Hz (Note 3)		1.5	4		2	5	$fA/\sqrt{Hz}$
	Input Voltage Range		±10.5	±11.5		±10.5	±11.5		V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = ±10.5V	84	98		82	97		dB
PSRR	Power Supply Rejection Ratio	V_S = ±9V to ±18V	88	102		86	101		dB
I_S	Supply Current			3.3	5.0		3.4	5.6	mA
V_O	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±13.0 ±12.0	±13.5 ±13.0		±13.0 ±12.0	±13.5 ±13.0		V V
BW	Bandwidth	G = 100 (Note 4) G = 10 (Note 4)	120 2.0	220 3.5		100 1.7	220 3.5		kHz MHz
SR	Slew Rate	G = 100, V_{IN} = ±0.13V, V_O = ±5V G = 10, V_{IN} = ±1V, V_O = ±5V	12 21	17 30		10 18	17 30		V/µs V/µs
	Overdrive Recovery	50% Overdrive (Note 5)		400			400		ns
	Settling Time	V_O = 20V Step (Note 4) G = 10 to 0.05% G = 10 to 0.01% G = 100 to 0.05% G = 100 to 0.01%		 1.8 3.0 7 9	 4.0 6.5 13 18		 1.8 3.0 7 9	 4.0 6.5 13 18	 µs µs µs µs

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $-55°C \le T_A \le 125°C$ for AM/M grades, $-40°C \le T_A \le 85°C$ for I grades, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM MIN	LT1102AM TYP	LT1102AM MAX	LT1102M/I MIN	LT1102M/I TYP	LT1102M/I MAX	UNITS
G_E	Gain Error	G = 100, $V_O = \pm 10V$, R_L = 50k or 2k G = 10, $V_O = \pm 10V$, R_L = 50k or 2k		0.10 0.05	0.25 0.12		0.10 0.06	0.30 0.15	% %
TCG_E	Gain Error Drift (Note 6)	G = 100, R_L = 50k or 2k G = 10, R_L = 50k or 2k		9 5	20 10		10 6	25 14	ppm/°C ppm/°C
G_{NL}	Gain Nonlinearity	G = 100, R_L = 50k G = 100, R_L = 2k G = 10, R_L = 50k or 2k		20 28 9	70 85 20		24 32 9	90 110 24	ppm ppm ppm
V_{OS}	Input Offset Voltage			300	1400		400	2000	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	µV/°C
I_{OS}	Input Offset Current			0.3	4		0.4	6	nA
I_B	Input Bias Current			±2	±10		±2.5	±15	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	82	97		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	88	100		84	99		dB
I_S	Supply Current	$T_A = 125°C$		2.5			2.5		mA
V_O	Maximal Output Voltage Swing	R_L = 50k R_L = 2k	±12.5 ±12.0	±13.2 ±12.6		±12.5 ±12.0	±13.2 ±12.6		V V

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AC MIN	LT1102AC TYP	LT1102AC MAX	LT1102C MIN	LT1102C TYP	LT1102C MAX	UNITS
G_E	Gain Error	G = 100, $V_O = \pm 10V$, R_L = 50k or 2k G = 10, $V_O = \pm 10V$, R_L = 50k or 2k		0.04 0.03	0.11 0.09		0.05 0.04	0.14 0.12	% %
TCG_E	Gain Error Drift (Note 6)	G = 100, R_L = 50k or 2k G = 10, R_L = 50k or 2k		8 5	18 10		9 6	22 14	ppm/°C ppm/°C
G_{NL}	Gain Nonlinearity	G = 100, R_L= 50k G = 100, R_L= 2k G = 10, R_L= 50k or 2k		8 11 8	30 36 18		9 12 8	40 48 22	ppm ppm ppm
V_{OS}	Input Offset Voltage			230	1000		280	1400	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	µV/°C
I_{OS}	Input Offset Current			10	150		15	220	pA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 6)		0.5	3		0.5	4	pA/°C
I_B	Input Bias Current			±40	±300		±50	±400	pA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 6)		1	4		1	6	pA/°C
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	83	98		81	97		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	87	101		85	100		dB
I_S	Supply Current	$T_A = 70°C$		2.8			2.9		mA
V_O	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±12.8 ±12.0	±13.4 ±12.8		±12.8 ±12.0	±13.4 ±12.8		V V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula:

$i_n = (2qI_B)^{1/2}$

where $q = 1.6 \bullet 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 4: This parameter is not tested. It is guaranteed by design and by inference from the slew rate measurement.

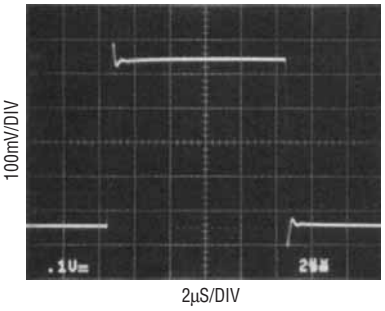
Note 5: Overdrive recovery is defined as the time delay from the removal of an input overdrive to the output's return from saturation to linear operation.

50% overdrive equals $V_{IN} = \pm 2V$ (G = 10) or $V_{IN} = \pm 200mV$ (G = 100).

Note 6: This parameter is not tested. It is guaranteed by design and by inference from other tests.

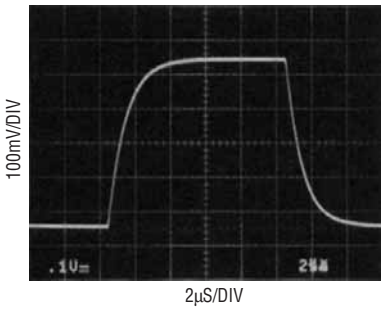
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Response, G = 10 (Input = 50mV Pulse)



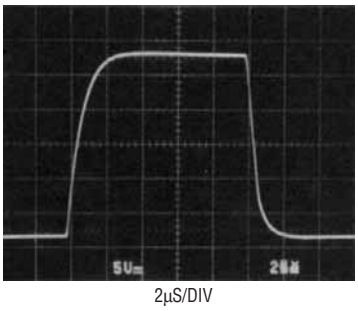
LT1102 • TPC01

Small Signal Response, G = 100 (Input = 5mV Pulse)



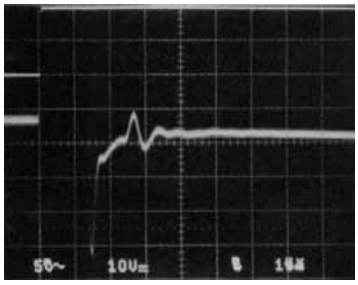
LT1102 • TPC02

Slew Rate, G = 100 (Input = ±130mV Pulse)



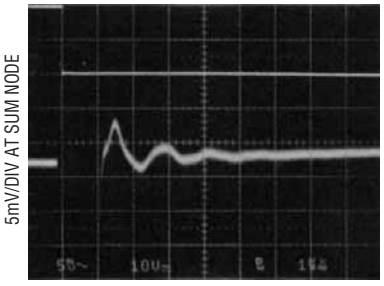
LT1102 • TPC03

Settling Time, G = 10 (Input From –10V to 10V)



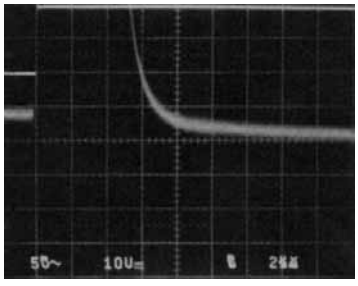
LT1102 • TPC04

Settling Time, G = 10 (Input From 10V to –10V)



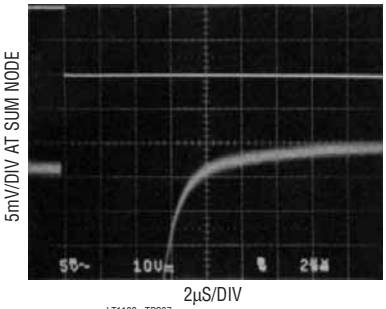
LT1102 • TPC05

Settling Time, G = 100 (Input From –10V to 10V)



LT1102 • TPC06

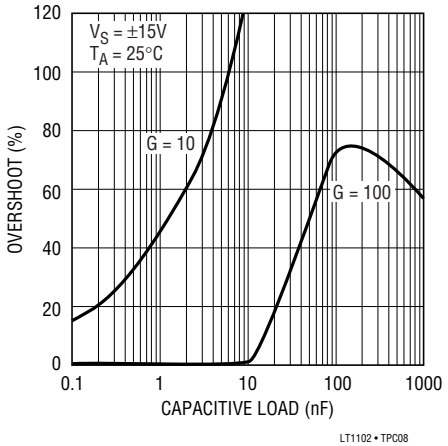
Settling Time, G = 100 (Input From 10V to –10V)



LT1102 • TPC07

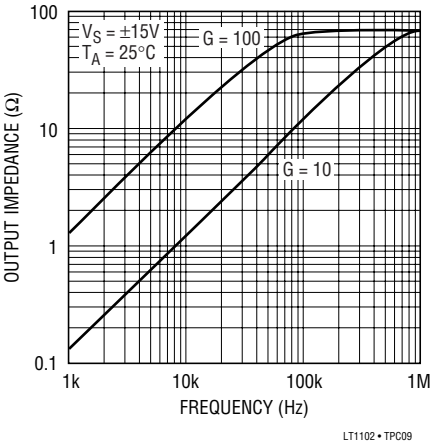
TYPICAL PERFORMANCE CHARACTERISTICS

Capacitive Load Handling



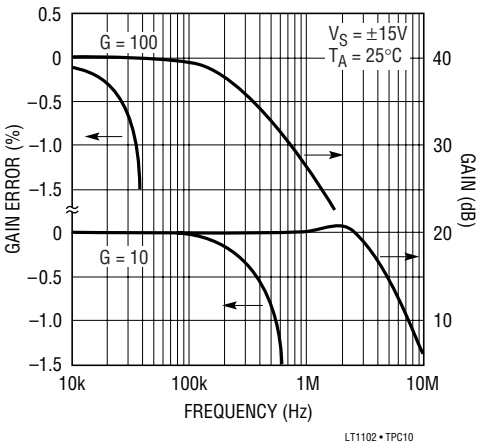
LT1102 • TPC08

Output Impedance vs Frequency



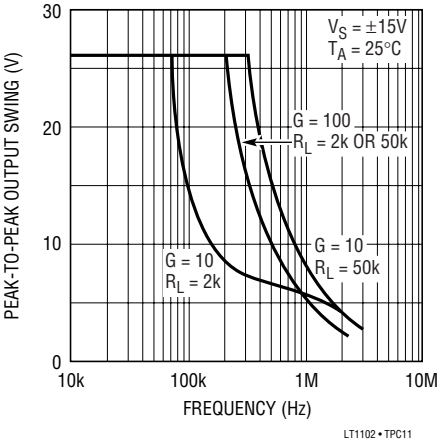
LT1102 • TPC09

Gain vs Frequency



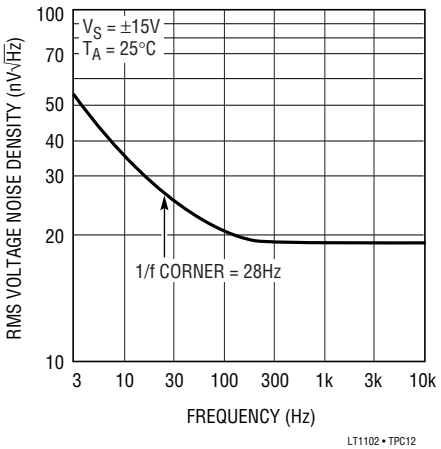
LT1102 • TPC10

Undistorted Output vs Frequency



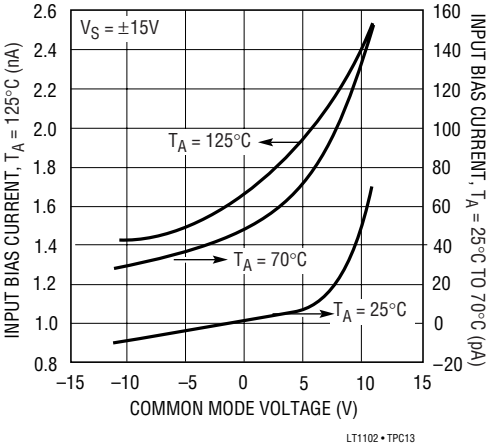
LT1102 • TPC11

Voltage Noise vs Frequency



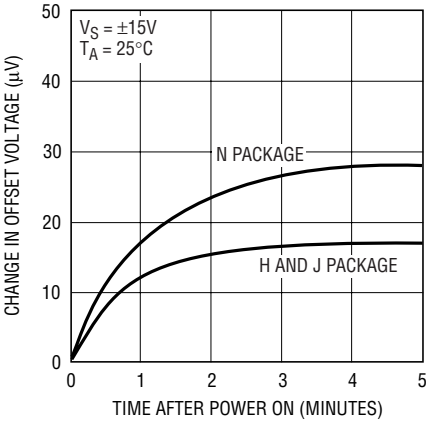
LT1102 • TPC12

Input Bias Current Over the Common Mode Range



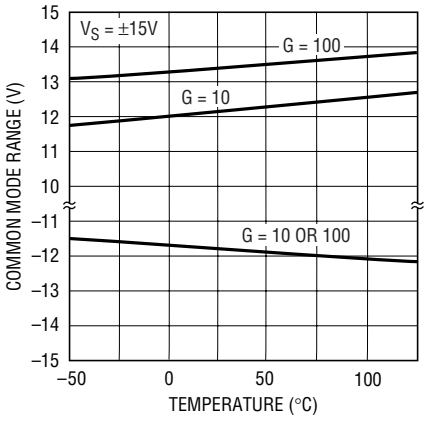
LT1102 • TPC13

Warm-Up Drift



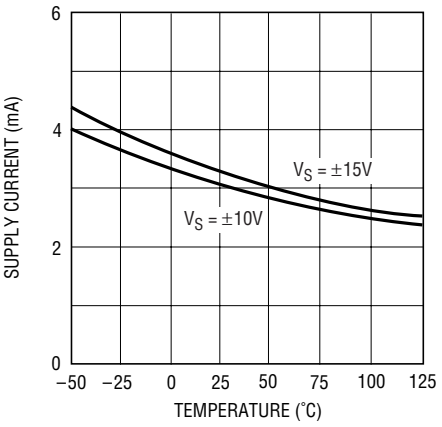
LT1102 • TPC14

Common Mode Range vs Temperature



LT1102 • TPC15

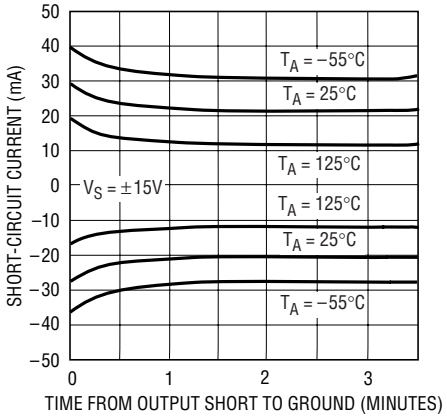
Supply Current vs Temperature



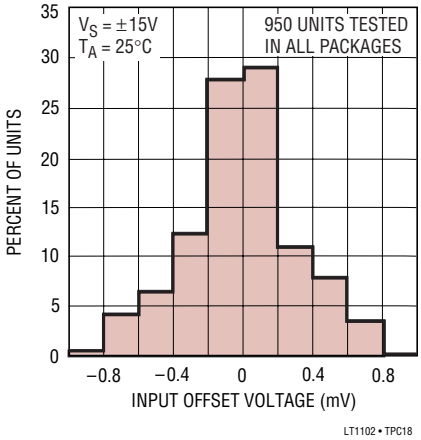
LT1102 • TPC16

TYPICAL PERFORMANCE CHARACTERISTICS

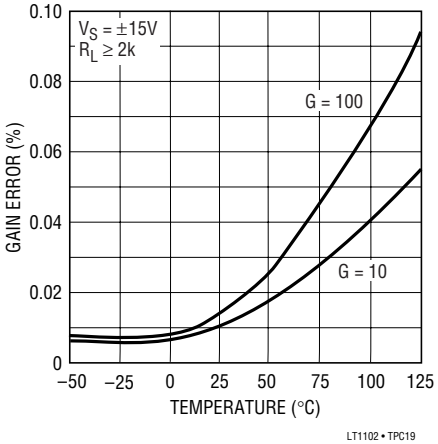
Short-Circuit Current vs Time



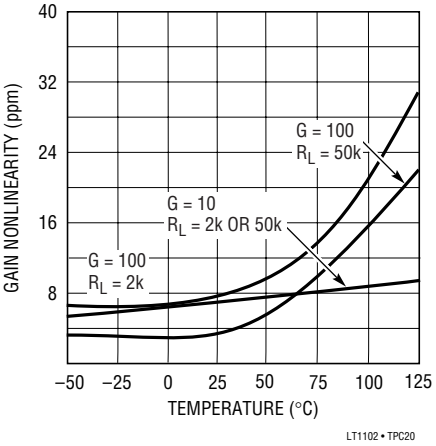
Distribution of Offset Voltage



Gain Error vs Temperature



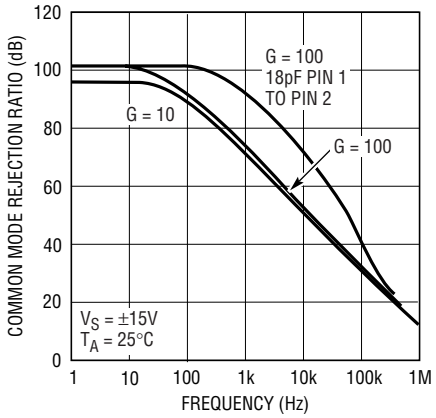
Gain Nonlinearity Over Temperature



APPLICATIONS INFORMATION

In the two op amp instrumentation amplifier configuration, the first amplifier is basically in unity gain, and the second amplifier provides all the voltage gain. In the LT1102, the second amplifier is decompensated for gain of 10 stability, therefore high slew rate and bandwidth are achieved. Common mode rejection versus frequency is also optimized in the G = 10 mode, because the bandwidths of the two op amps are similar. When G = 100, this statement is no longer true; however, by connecting an 18pF capacitor between pins 1 and 2, a common mode AC gain is created to cancel the inherent roll-off. From 200Hz to 30kHz, CMRR versus frequency is improved by an order of magnitude.

Common Mode Rejection Ratio vs Frequency



Input Protection

Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1102 employs FET input transistors, consequently the differential input voltage can be ±30V (with ±15V supplies, ±36V with ±18V supplies). Some competitive instrumentation amplifiers have NPN inputs which are protected by back-to-back diodes. When the differential input Voltage exceeds ±13V on these competitive devices, input current increases to milliampere level; more than ±10V differential voltage can cause permanent damage.

When the LT1102 inputs are pulled below the negative supply or above the positive supply, the inputs will clamp a diode voltage below or above the supplies. No damage will occur if the input current is limited to 20mA.

Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors (= R_X) between pins 1 and 2 and pins 7 and 8.

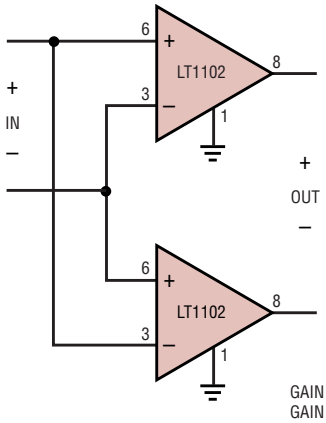
$$\text{Gain} = 10 + \frac{R_X}{R + R_X/90}$$

The nominal value of R is 1.84kΩ. The usefulness of this method is limited by the fact that R is not controlled to better than ±10% absolute accuracy in production. However, on any specific unit, 90R can be measured between Pins 1 and 2.

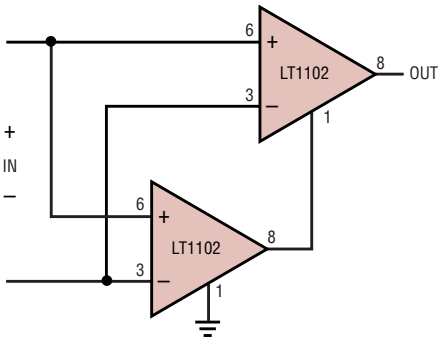
APPLICATIONS INFORMATION

Gain = 20, 110, or 200 Instrumentation Amplifiers

Differential Output



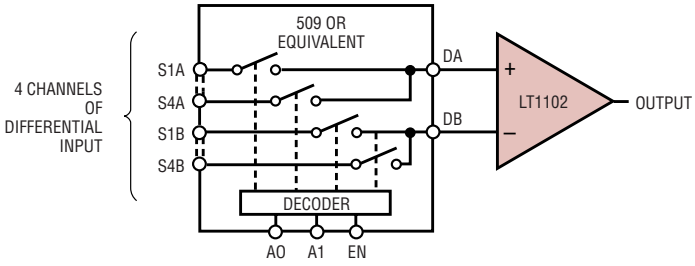
Single Ended Output



GAIN = 200, AS SHOWN
GAIN = 20, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON BOTH DEVICES
GAIN = 110, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON ONE DEVICE, NOT ON THE OTHER
INPUT REFERRED NOISE IS REDUCED BY √2 (G = 200 OR 20)

LT1102 • AI02

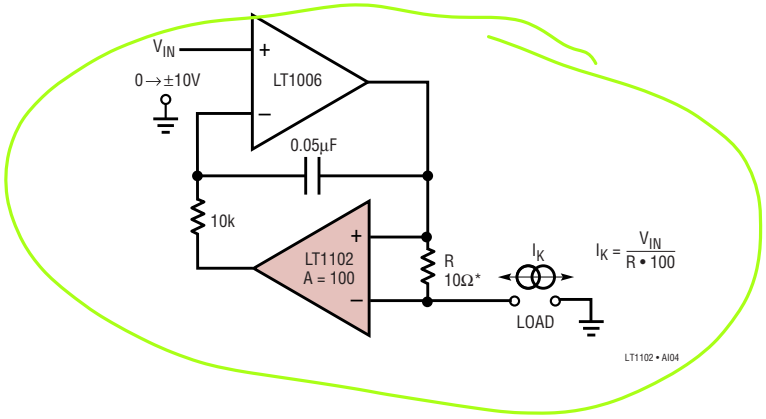
Multiplexed Input Data Acquisition



800kHz SIGNALS CAN BE MULTIPLEXED WITH LT1102 IN G = 10

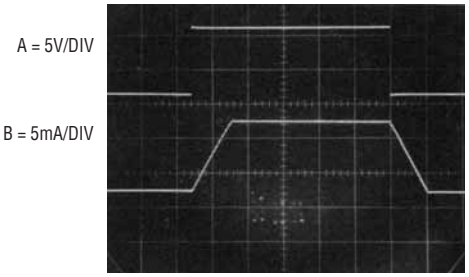
LT1102 • AI03

Voltage Programmable Current Source is Simple and Precise



LT1102 • AI04

Dynamic Response of the Current Source

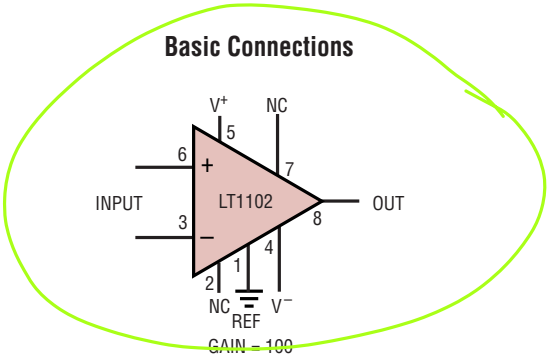


HORIZ. = 20µs/DIV

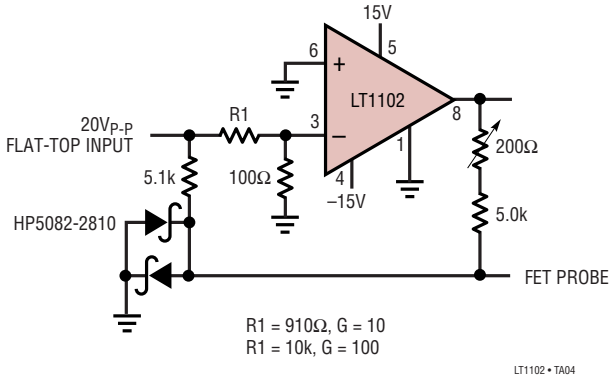
LT1102 • AI05

TYPICAL APPLICATIONS

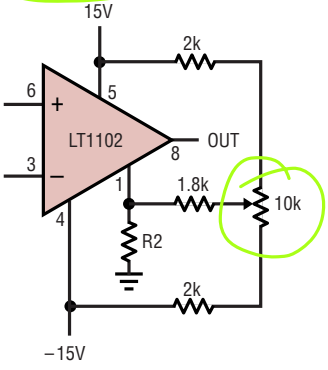
Basic Connections



Settling Time Test Circuit

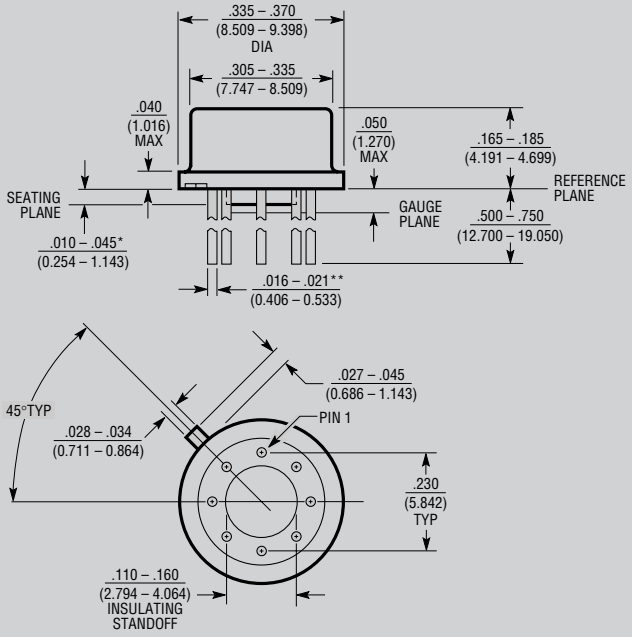


Offset Nulling



PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.230 Inch PCD)
(Reference LTC DWG # 05-08-1321)

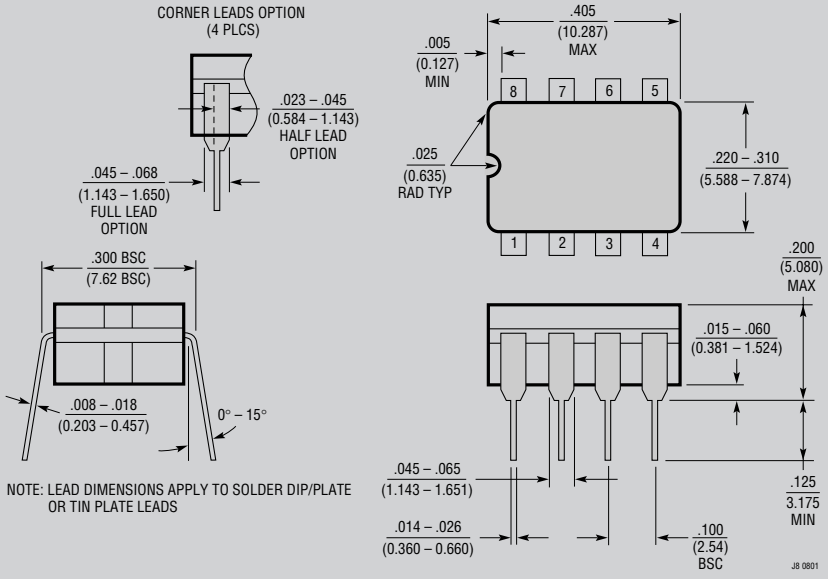


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS .016 – .024 (0.406 – 0.610)

H8 (TO-5) 0.230 PCD 0801

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

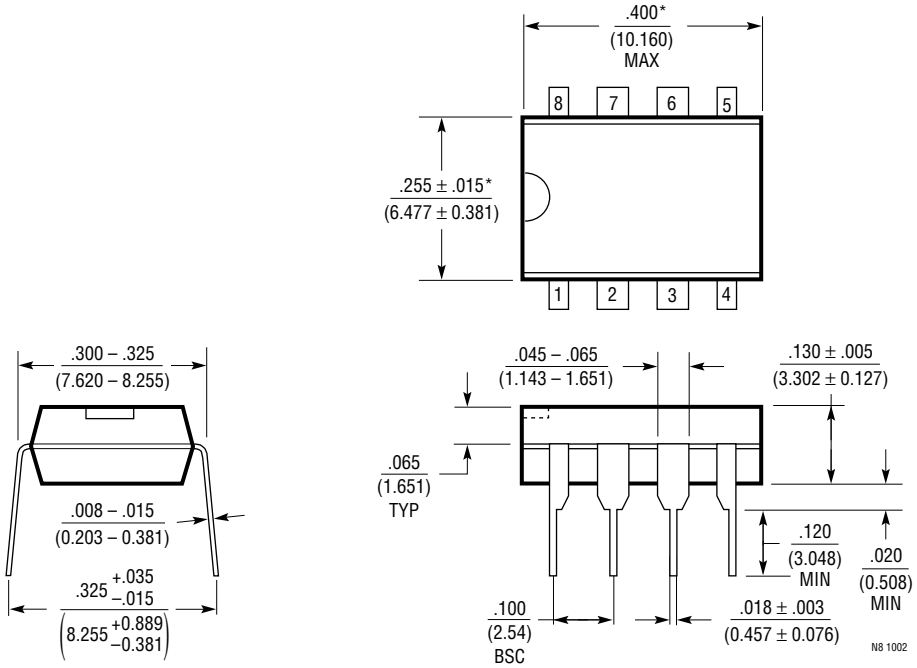


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

OBSOLETE PACKAGES

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

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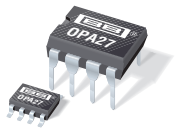


SBOS135C – JANUARY 1984 – REVISED AUGUST 2005

Ultra-Low Noise, Precision OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: 4.5nV/√Hz max at 1kHz
- LOW OFFSET: 100μV max
- LOW DRIFT: 0.4μV/°C
- HIGH OPEN-LOOP GAIN: 117dB min
- HIGH COMMON-MODE REJECTION: 100dB min
- HIGH POWER-SUPPLY REJECTION: 94dB min
- FITS OP-07, OP-05, AD510, AND AD517 SOCKETS

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIERS
- RADIATION HARD EQUIPMENT

DESCRIPTION

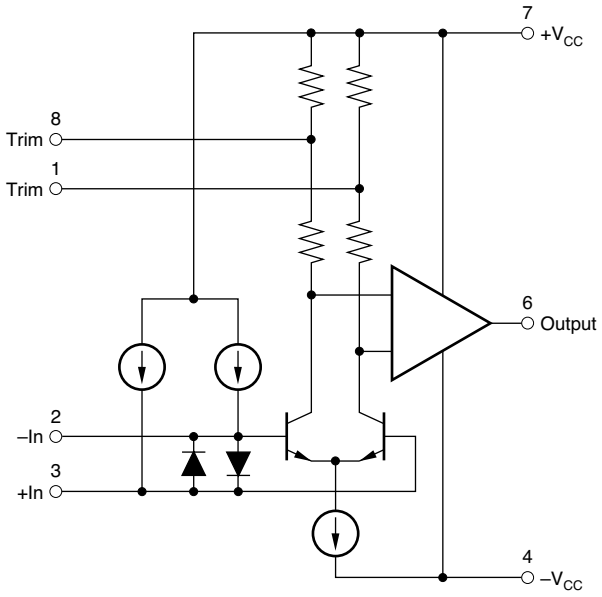
The OPA27 and OPA37 are ultra-low noise, high-precision monolithic operational amplifiers.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full –40°C to +85°C temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5.

The Texas Instruments' OPA27 and OPA37 are improved replacements for the industry-standard OP-27 and OP-37.



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±22V
Internal Power Dissipation (2)	500mW
Input Voltage	$\pm V_{CC}$
Output Short-Circuit Duration (3)	Indefinite
Differential Input Voltage (4)	±0.7V
Differential Input Current (4)	±25mA
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature:	
P (soldering, 10s)	+300°C
U (soldering, 3s)	+260°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Maximum package power dissipation versus ambient temperature. (2) To common with $\pm V_{CC}$ = 15V. (4) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	θ_{JA}	PACKAGE DRAWING	PACKAGE MARKING
OPA27	DIP-8	100°C/W	P	OPA27GP
OPA27	SO-8	160°C/W	D	OPA27U
OPA37	DIP-8	100°C/W	P	OPA37GP
OPA37	SO-8	160°C/W	D	OPA37U

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

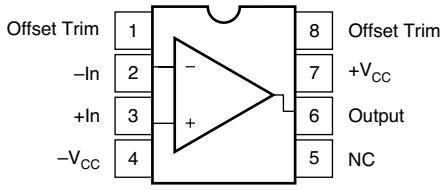
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View



NC = No Connection

ELECTRICAL CHARACTERISTICS

At V_{CC} = ±15V and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA27 OPA37 MIN	OPA27 OPA37 TYP	OPA27 OPA37 MAX	UNITS
INPUT NOISE (6)					
Voltage, f_O = 10Hz			3.8	8.0	nV/√Hz
f_O = 30Hz			3.3	5.6	nV/√Hz
f_O = 1kHz			3.2	4.5	nV/√Hz
f_B = 0.1Hz to 10Hz			0.09	0.25	μV_{PP}
Current,(1) f_O = 10Hz			1.7		pA/√Hz
f_O = 30Hz			1.0		pA/√Hz
f_O = 1kHz			0.4	0.6	pA/√Hz
OFFSET VOLTAGE (2)					
Input Offset Voltage			±25	±100	µV
Average Drift (3)	$T_{A\,MIN}$ to $T_{A\,MAX}$		±0.4	±1.8 (6)	µV/°C
Long Term Stability (4)			0.4	2.0	µV/mo
Supply Rejection	±V_{CC} = 4 to 18V	94	120		dB
	±V_{CC} = 4 to 18V		±1	±20	µV/V
BIAS CURRENT					
Input Bias Current			±15	±80	nA
OFFSET CURRENT					
Input Offset Current			10	75	nA
IMPEDANCE					
Common-Mode			2 ll 2.5		GΩ ll pF
VOLTAGE RANGE					
Common-Mode Input Range		±11	±12.3		V
Common-Mode Rejection	V_{IN} = ±11VDC	100	122		dB
OPEN-LOOP VOLTAGE GAIN, DC	R_L ≥ 2kΩ	117	124		dB
	R_L ≥ 1kΩ		124		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product (5)	OPA27	5 (6)	8		MHz
	OPA37	45 (6)	63		MHz
Slew Rate (5)	V_O = ±10V, R_L = 2kΩ				
	OPA27, G = +1	1.7 (6)	1.9		V/µs
	OPA37, G = +5	11 (6)	11.9		V/µs
Settling Time, 0.01%	OPA27, G = +1		25		µs
	OPA37, G = +5		25		µs
RATED OUTPUT					
Voltage Output	R_L ≥ 2kΩ	±12	±13.8		V
	R_L ≥ 600Ω	±10	±12.8		V
Output Resistance	DC, Open Loop		70		Ω
Short Circuit Current	R_L = 0Ω		25	60 (6)	mA
POWER SUPPLY					
Rated Voltage			±15		VDC
Voltage Range, Derated Performance		±4		±22	VDC
Current, Quiescent	I_O = 0mADC		3.3	5.7	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operating		–40		+85	°C

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specification are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter specified by design.

ELECTRICAL CHARACTERISTICS (Cont.)

At V_{CC} = ±15V and –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

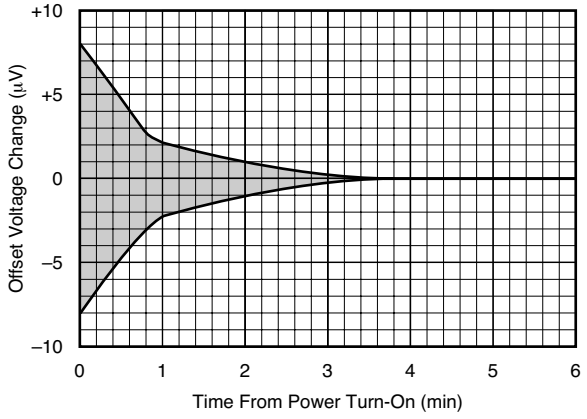
PARAMETER	CONDITIONS	OPA27 OPA37 MIN	OPA27 OPA37 TYP	OPA27 OPA37 MAX	UNITS
INPUT VOLTAGE(1)					
Input Offset Voltage			±48	±220(3)	µV
Average Drift(2)	$T_{A\ MIN}$ to $T_{A\ MAX}$		±0.4	±1.8(3)	µV/°C
Supply Rejection	±V_{CC} = 4.5 to 18V				
	±V_{CC} = 4.5 to 18V	90 (3)	122		dB
BIAS CURRENT					
Input Bias Current			±21	±150(3)	nA
OFFSET CURRENT					
Input Offset Current			20	135(3)	nA
VOLTAGE RANGE					
Common-Mode Input Range		±10.5(3)	±11.8		V
Common-Mode Rejection	V_{IN} = ±11VDC	96(3)	122		dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain	R_L ≥ 2kΩ	113(3)	120		dB
RATED OUTPUT					
Voltage Output	R_L = 2kΩ	±11.0(3)	±13.4		V
Short Circuit Current	V_O = 0VDC		25		mA
TEMPERATURE RANGE					
Specification		–40		+85	°C

NOTES: (1) Offset voltage specification are measured with automatic test equipment after approximately 0.5s from power turn-on. (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (3) This parameter specified by design.

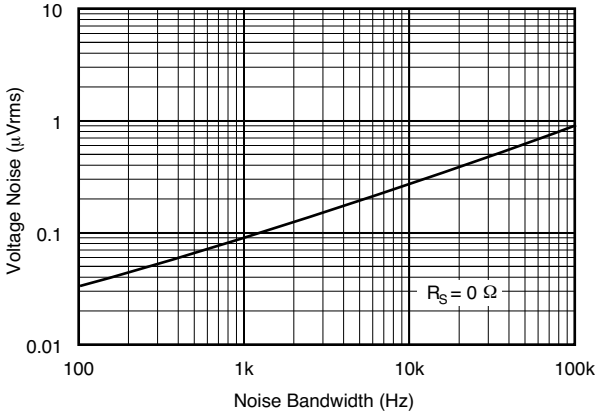
TYPICAL CHARACTERISTICS

At T_A = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

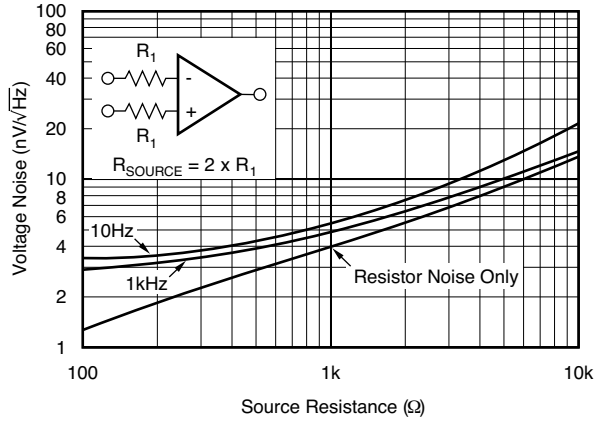
INPUT OFFSET VOLTAGE WARM-UP DRIFT



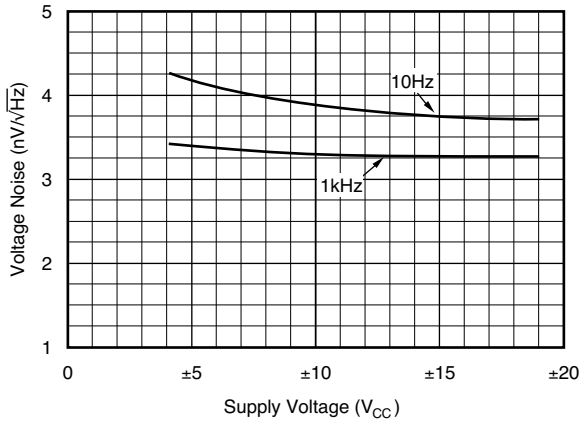
INPUT VOLTAGE NOISE vs NOISE BANDWIDTH
(0.1Hz to Indicated Frequency)



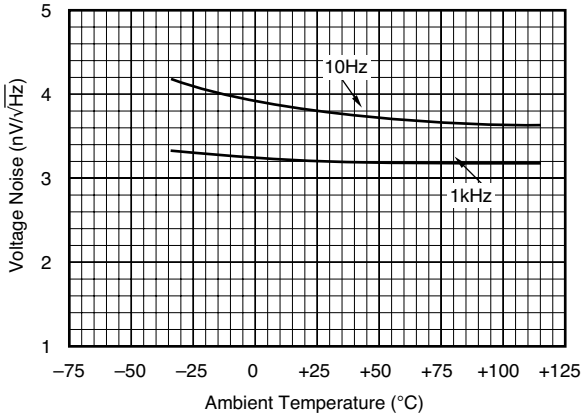
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
vs SOURCE RESISTANCE



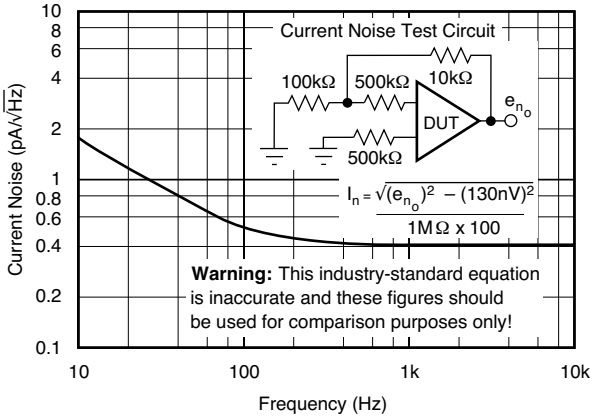
VOLTAGE NOISE SPECTRAL DENSITY
vs SUPPLY VOLTAGE



VOLTAGE NOISE SPECTRAL DENSITY
vs TEMPERATURE



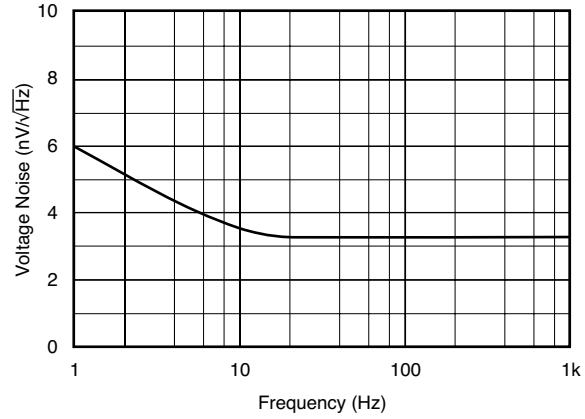
INPUT CURRENT NOISE SPECTRAL DENSITY



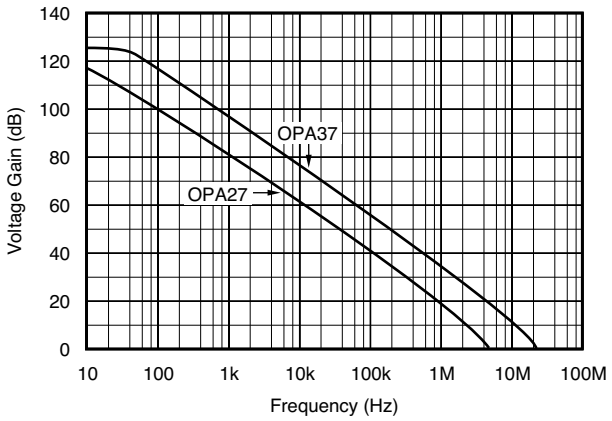
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

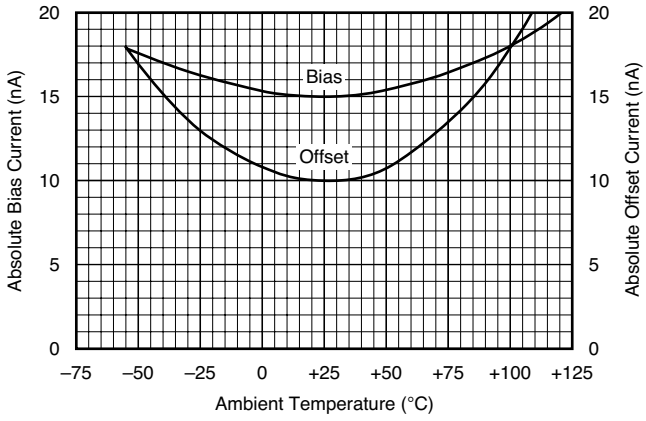
INPUT VOLTAGE NOISE SPECTRAL DENSITY



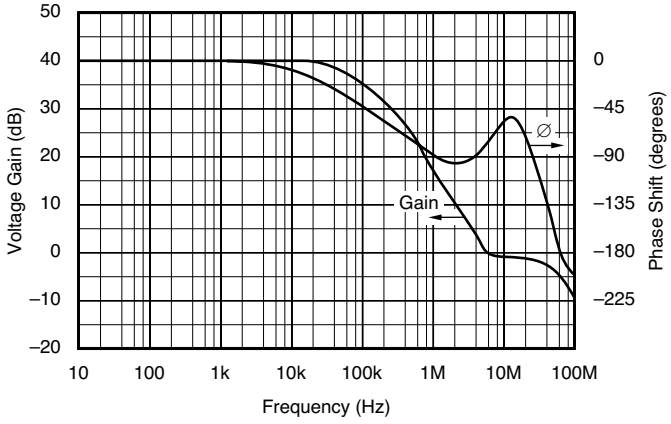
OPEN-LOOP FREQUENCY RESPONSE



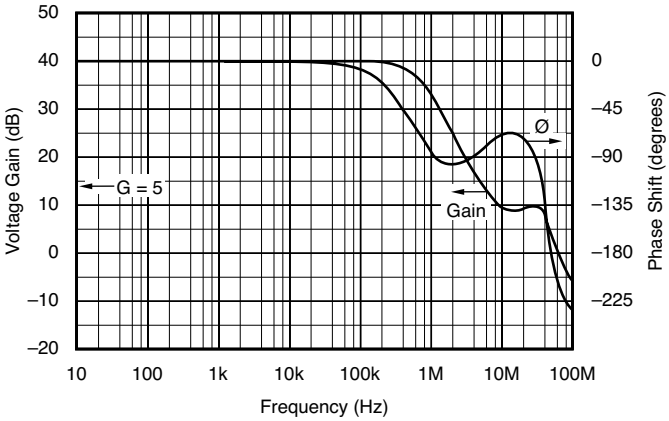
BIAS AND OFFSET CURRENT vs TEMPERATURE



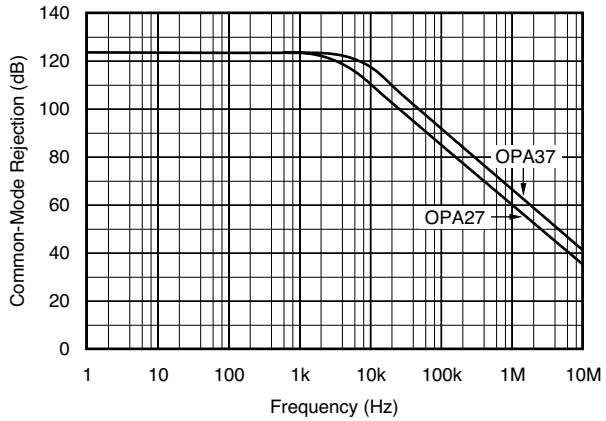
OPA27 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



OPA37 CLOSED-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY (G = 100)



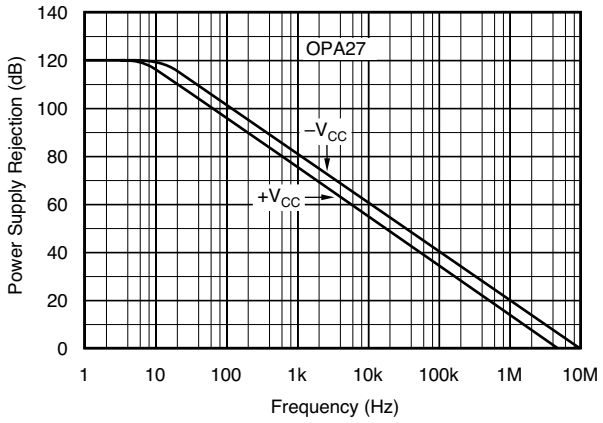
COMMON-MODE REJECTION vs FREQUENCY



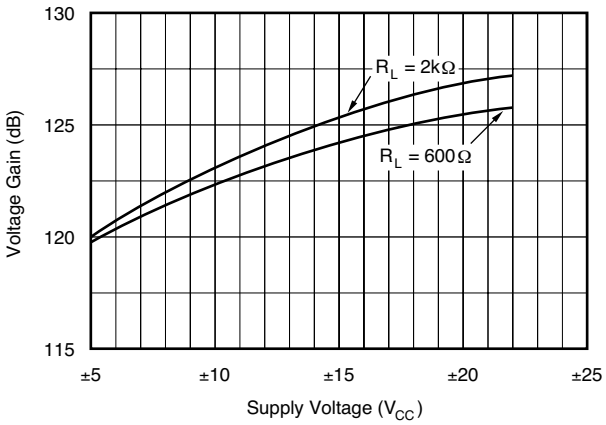
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

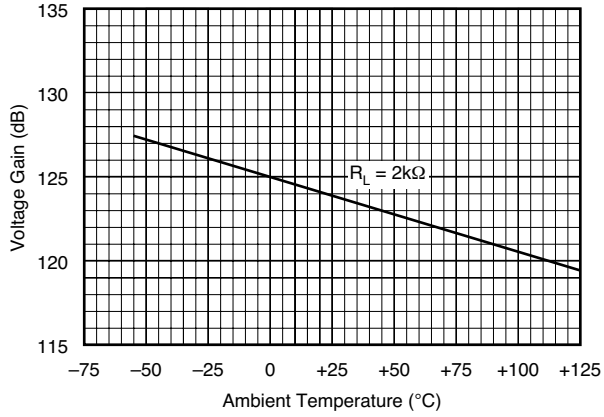
POWER SUPPLY REJECTION vs FREQUENCY



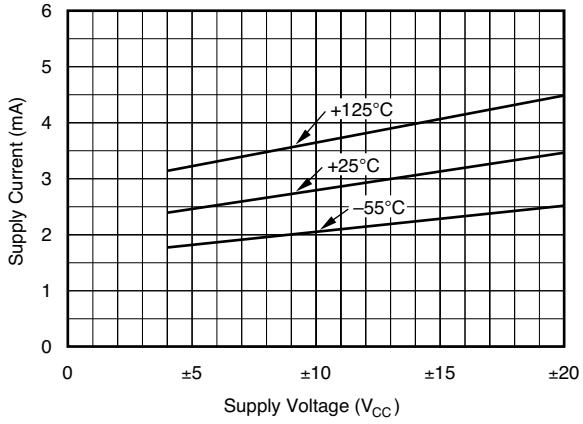
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



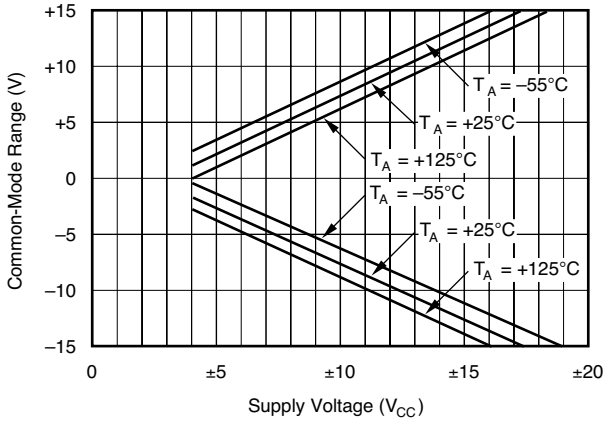
OPEN-LOOP VOLTAGE GAIN vs TEMPERATURE



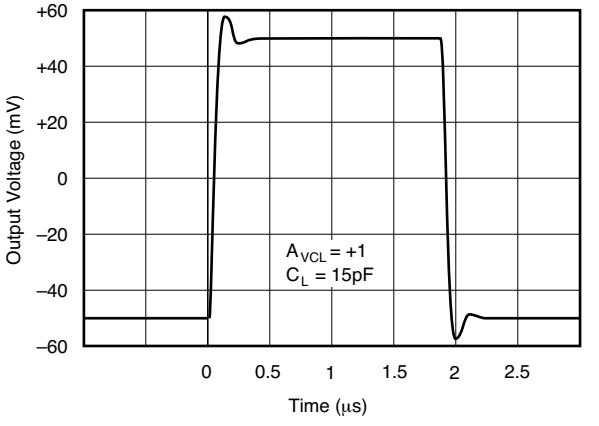
SUPPLY CURRENT vs SUPPLY VOLTAGE



COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



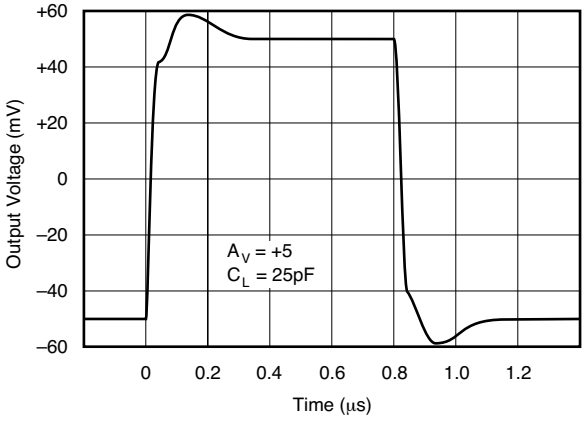
OPA27 SMALL SIGNAL TRANSIENT RESPONSE



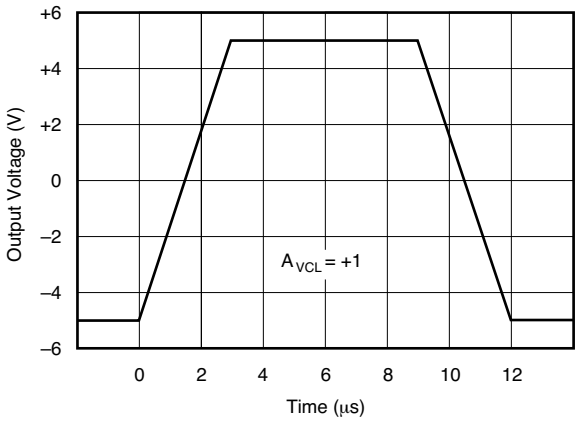
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, $\pm V_{CC}$ = ±15VDC, unless otherwise noted.

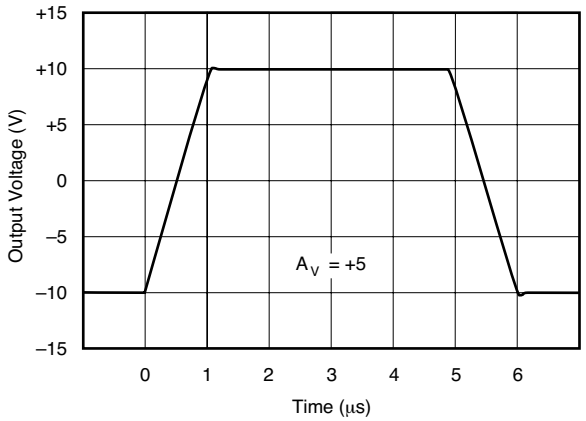
OPA37 SMALL SIGNAL TRANSIENT RESPONSE



OPA27 LARGE SIGNAL TRANSIENT RESPONSE



OPA37 LARGE SIGNAL TRANSIENT RESPONSE



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA27 and OPA37 offset voltages are laser-trimmed and require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used, but V_{OS} drift will be degraded by an additional 0.1μV/°C to 0.2μV/°C. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 3.3μV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very small offsets, the higher resolution circuit shown in Figure 4 is recommended.

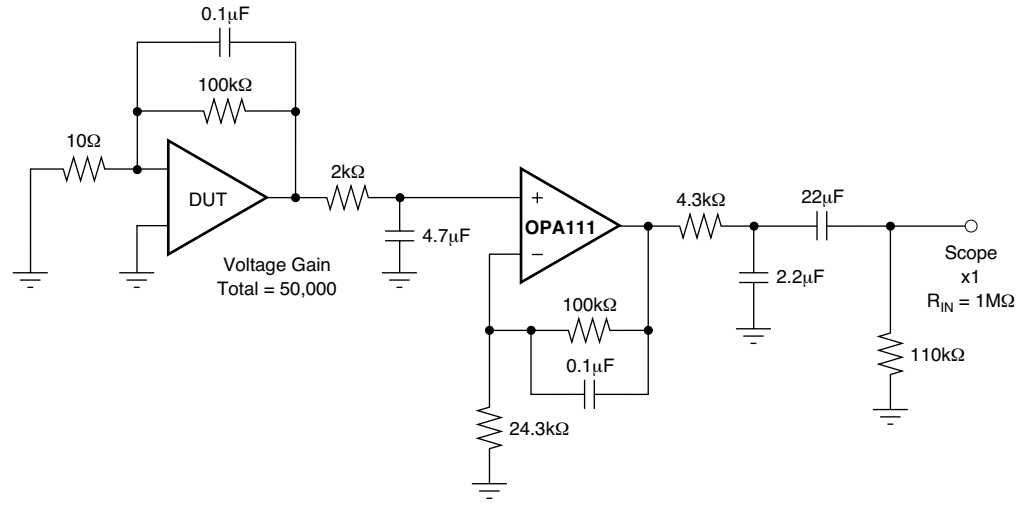
The OPA27 and OPA37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

THERMOELECTRIC POTENTIALS

The OPA27 and OPA37 are laser-trimmed to microvolt-level input offset voltages, and for very-low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMFs if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference (see Figure 11).

Short, direct mounting of the OPA27 and OPA37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.



NOTE: All capacitor values are for nonpolarized capacitors only.

FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

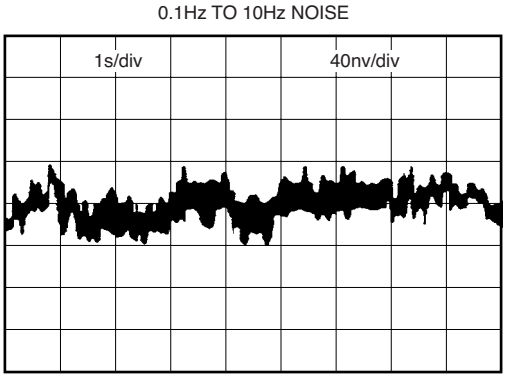


FIGURE 2. Low Frequency Noise.

NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ, the OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27, as shown in Figure 5.

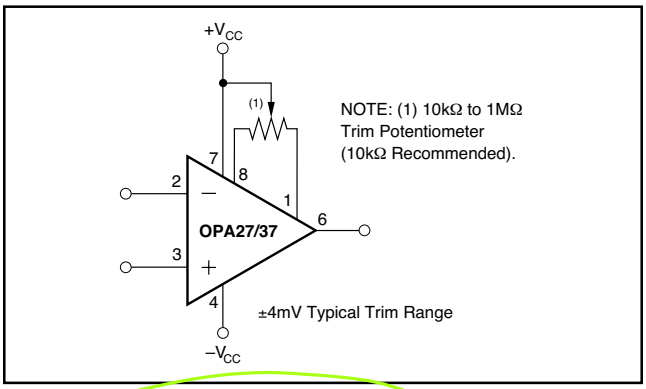


FIGURE 3. Offset Voltage Trim.

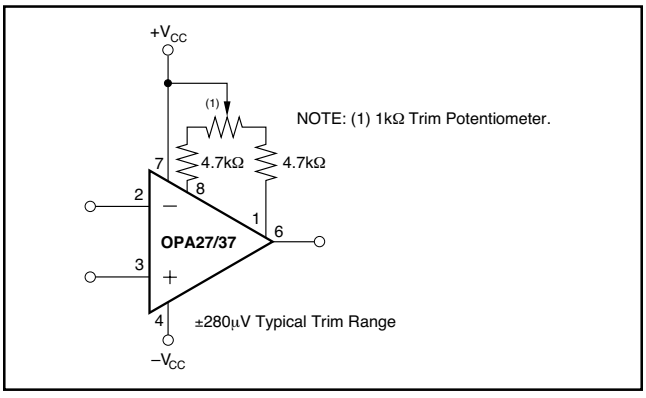


FIGURE 4. High Resolution Offset Voltage Trim.

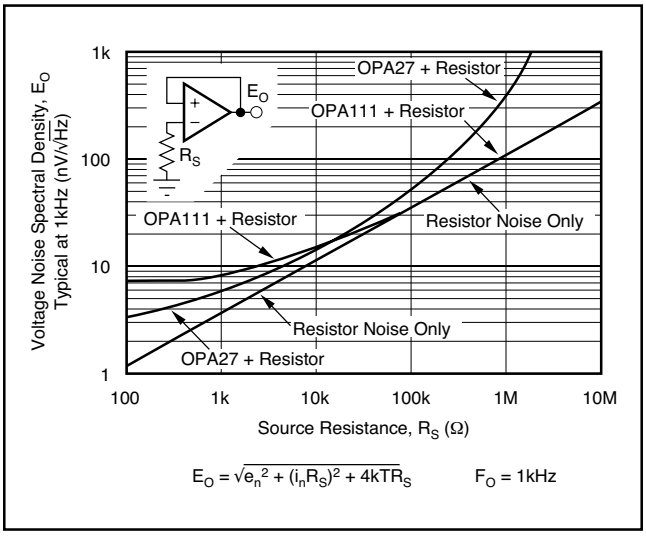


FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_F) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_F and C_{IN} and eliminate peaking or oscillation.

INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27 and OPA37. Exceeding a few hundred millivolts differential input signal will cause current to flow, and without external current limiting resistors, the input will be destroyed.

Accidental static discharge, as well as high current, can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged, as will any precision operational amplifier subjected to this abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew rate. When using the OPA27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended, as shown in Figure 6.

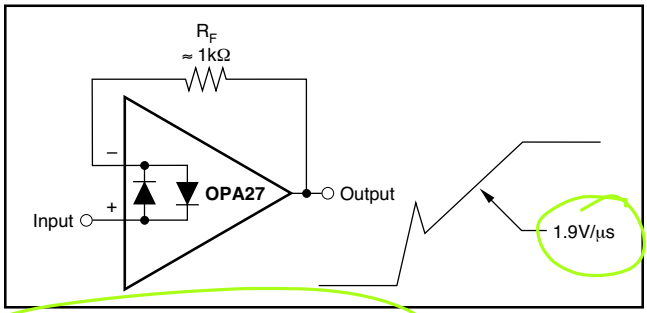


FIGURE 6. Pulsed Operation.

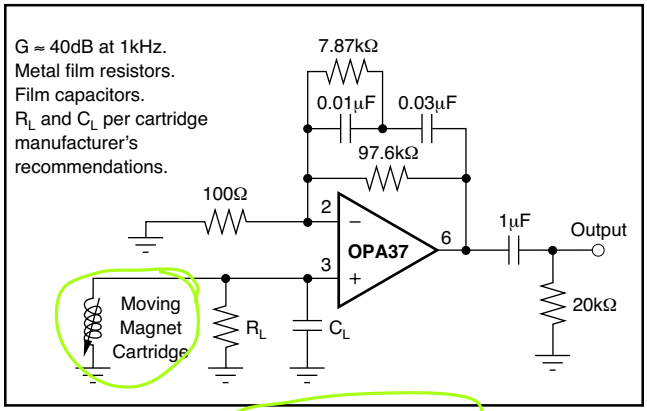


FIGURE 7. Low-Noise RIAA Preamplifier.

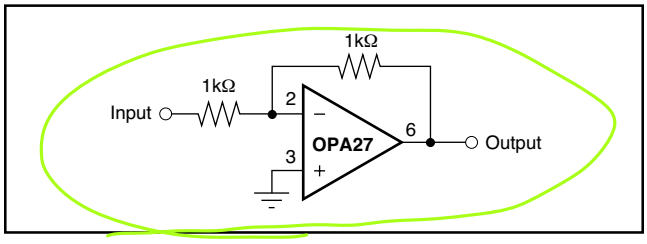


FIGURE 8. Unity-Gain Inverting Amplifier.

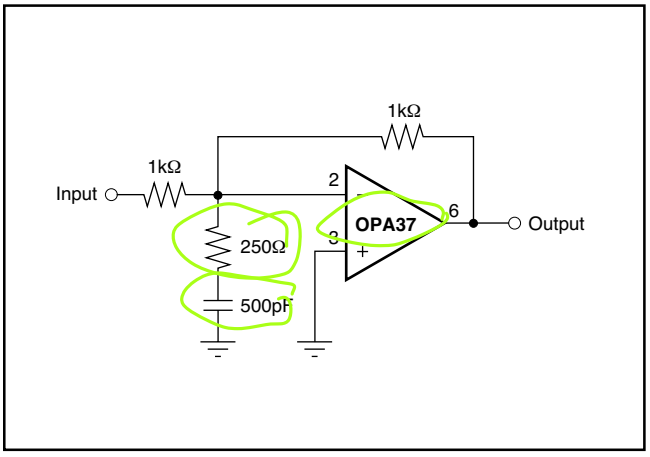


FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

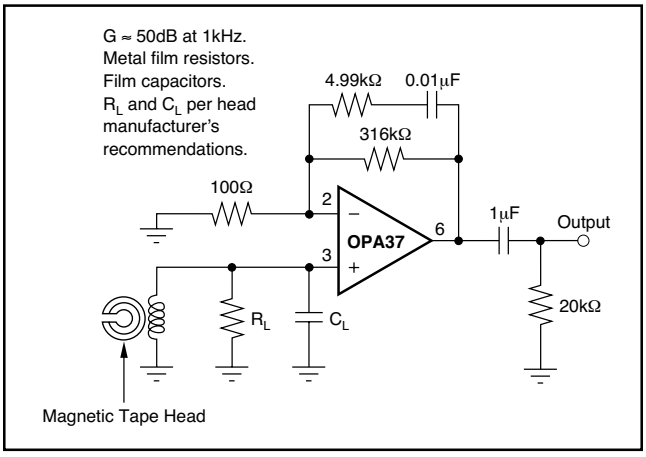


FIGURE 10. NAB Tape Head Preamplifier.

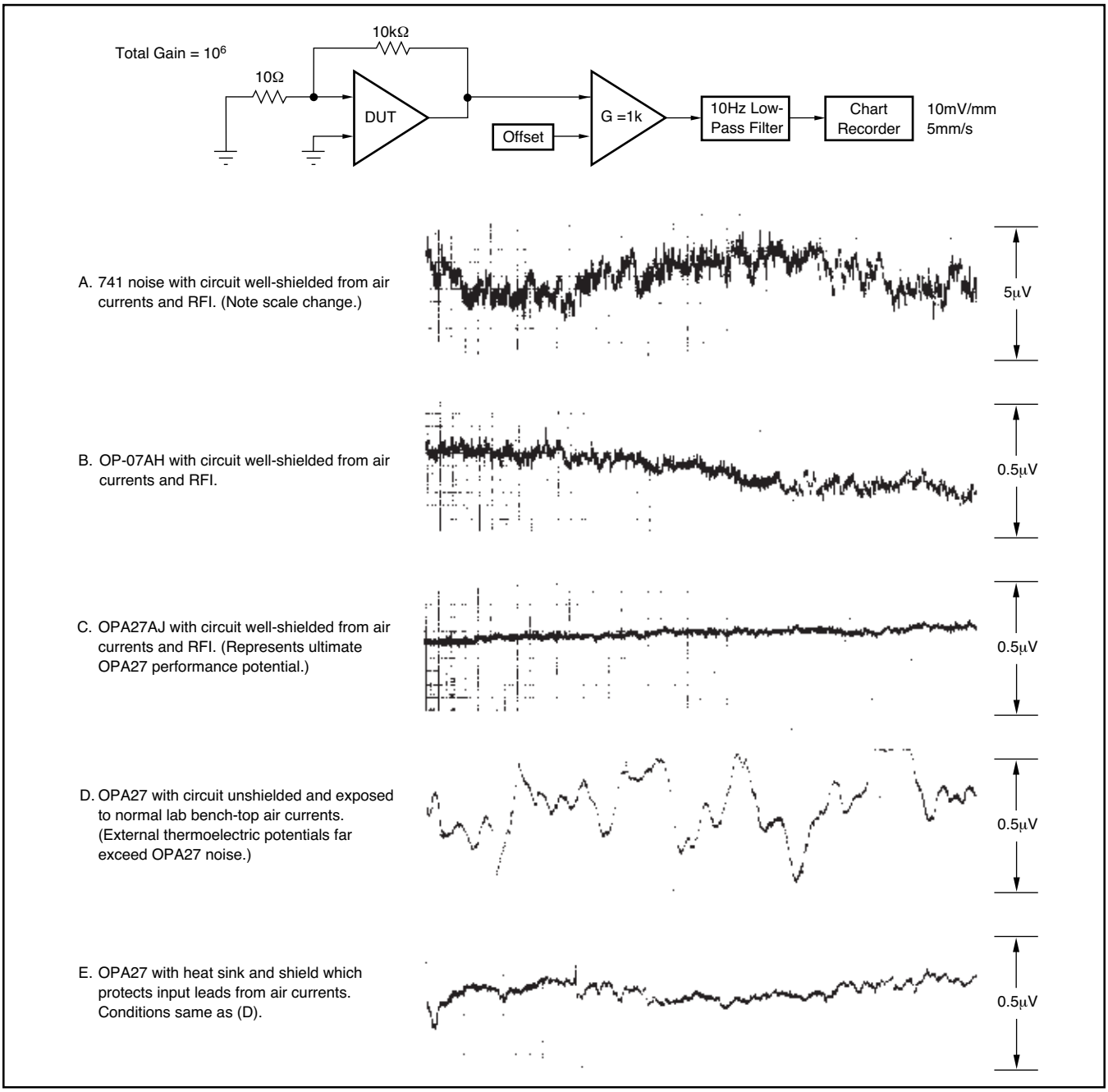


FIGURE 11. Low Frequency Noise Comparison.

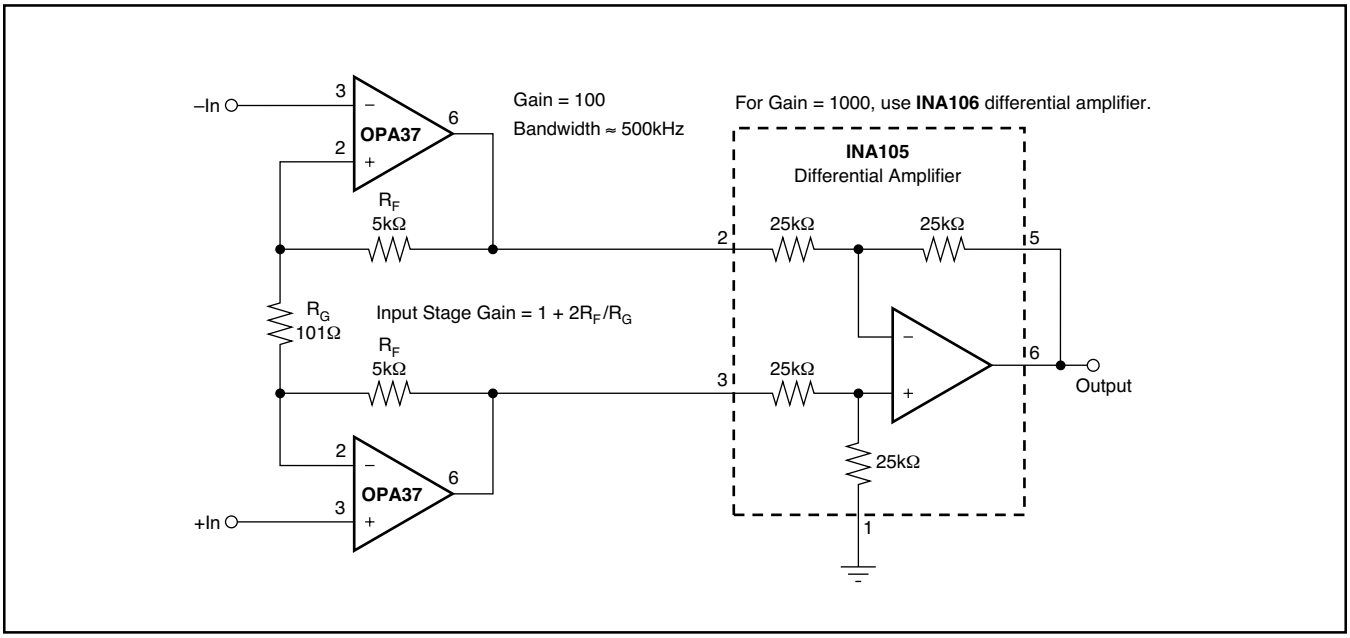


FIGURE 12. Low Noise Instrumentation Amplifier.

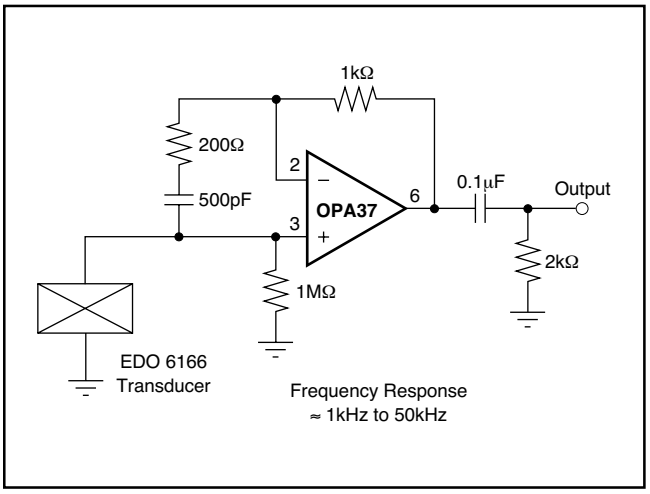


FIGURE 13. Hydrophone Preamplifier.

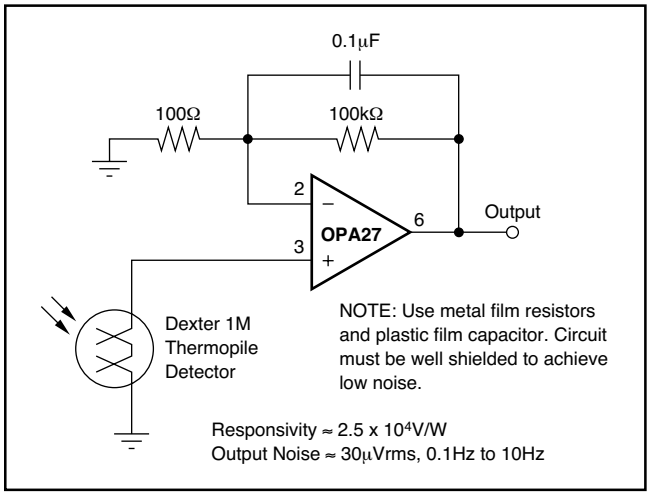


FIGURE 14. Long-Wavelength Infrared Detector Amplifier.

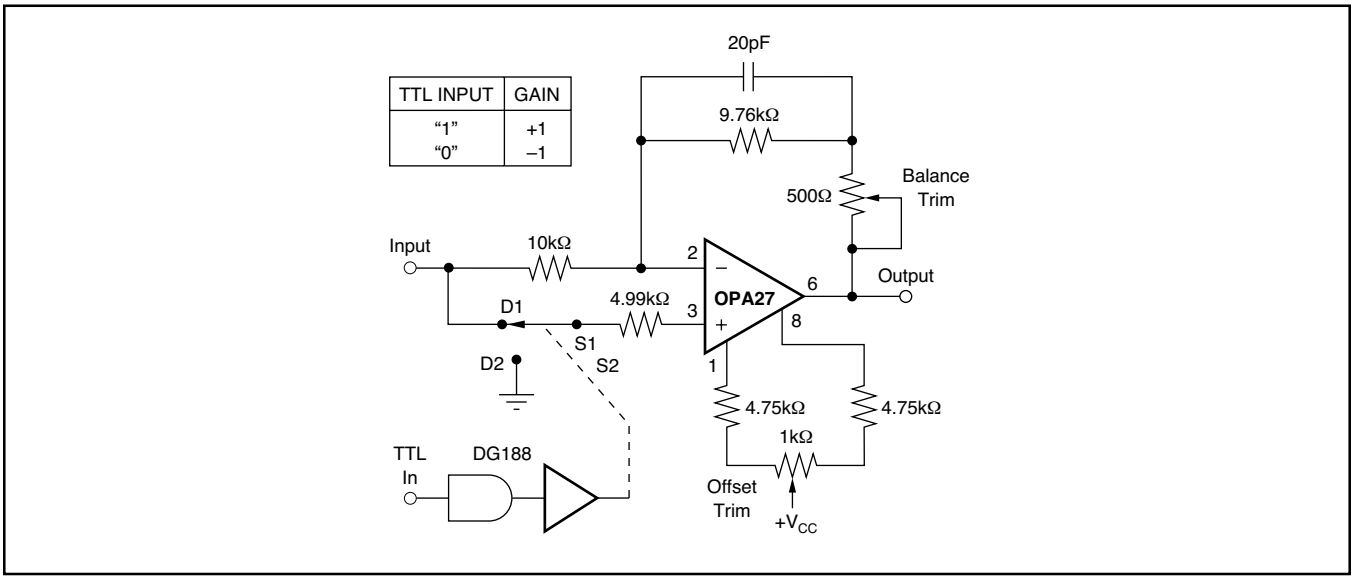


FIGURE 15. High Performance Synchronous Demodulator.

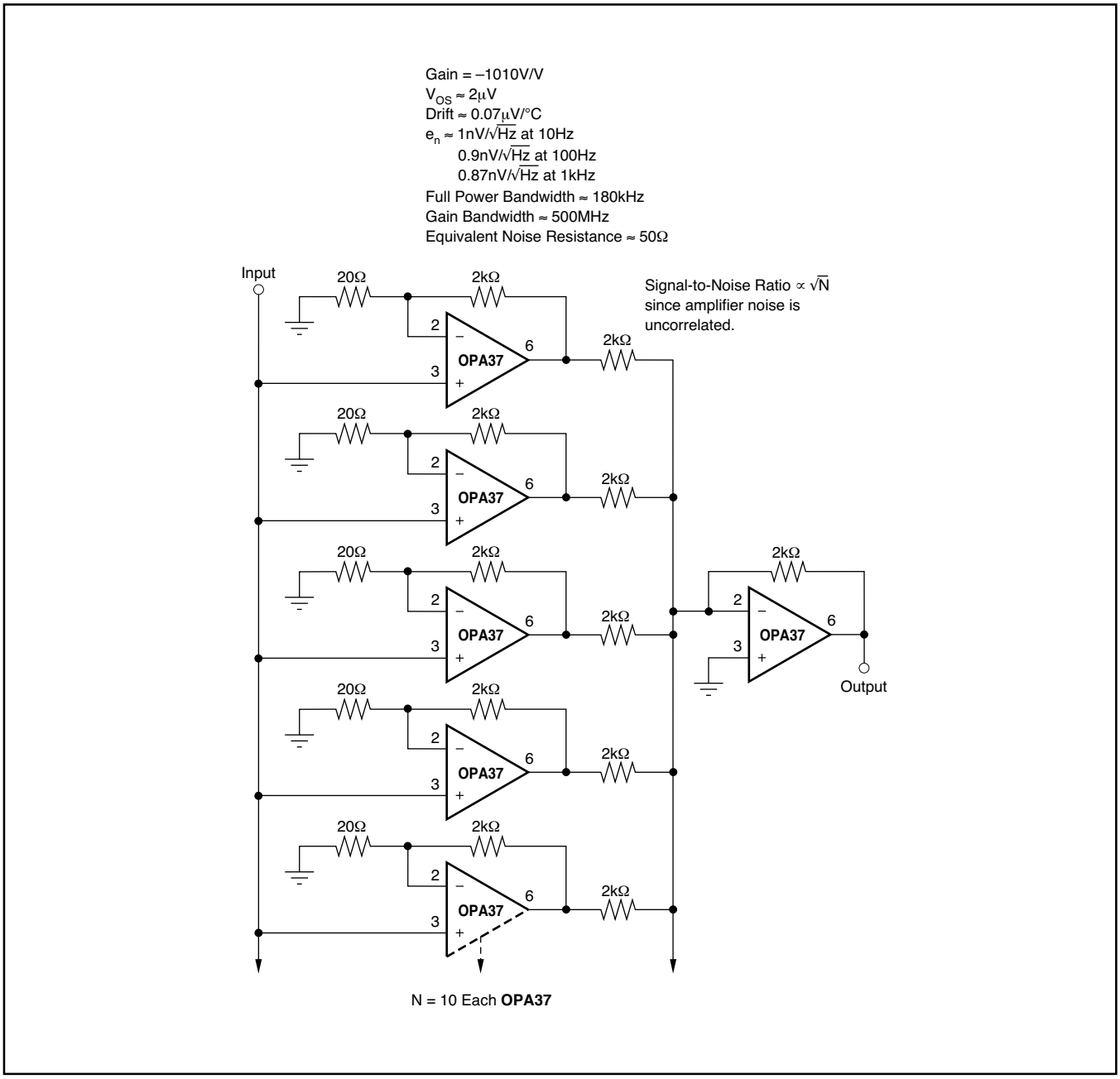


FIGURE 16. Ultra-Low Noise “N”-Stage Parallel Amplifier.

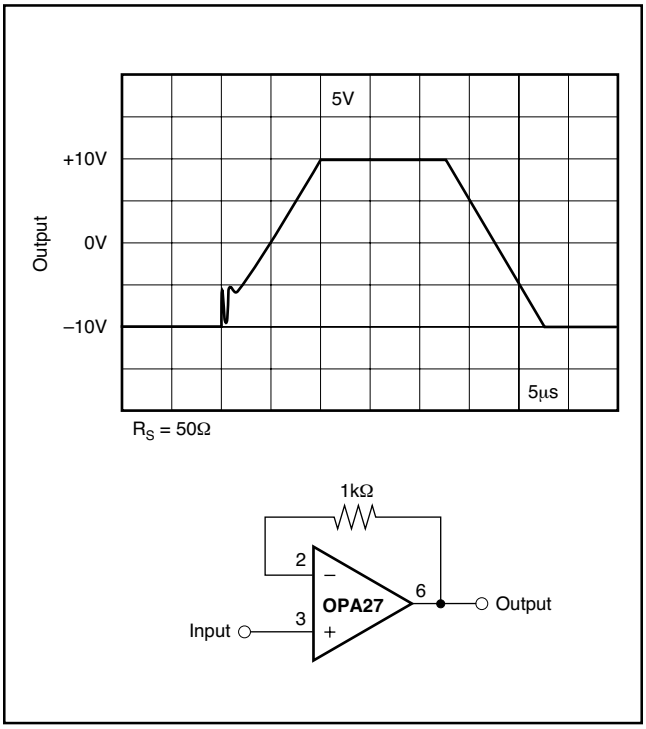


FIGURE 17. Unity-Gain Buffer.

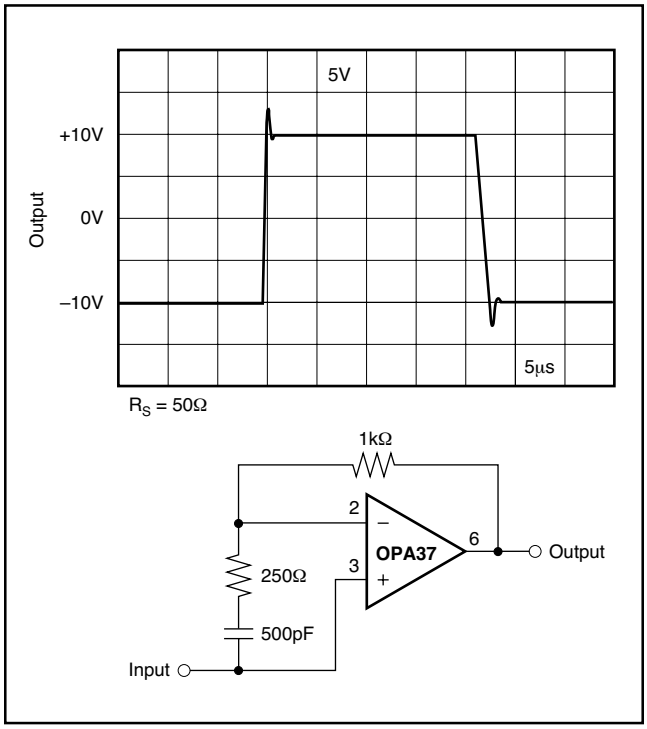


FIGURE 18. High Slew Rate Unity-Gain Buffer.

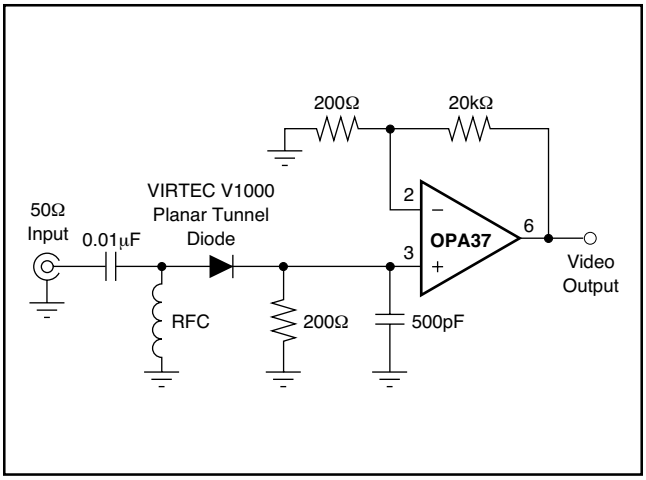


FIGURE 19. RF Detector and Video Amplifier.

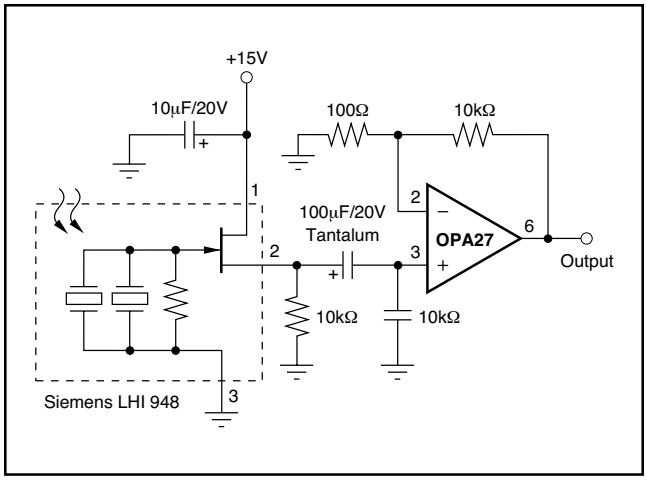


FIGURE 20. Balanced Pyroelectric Infrared Detector.

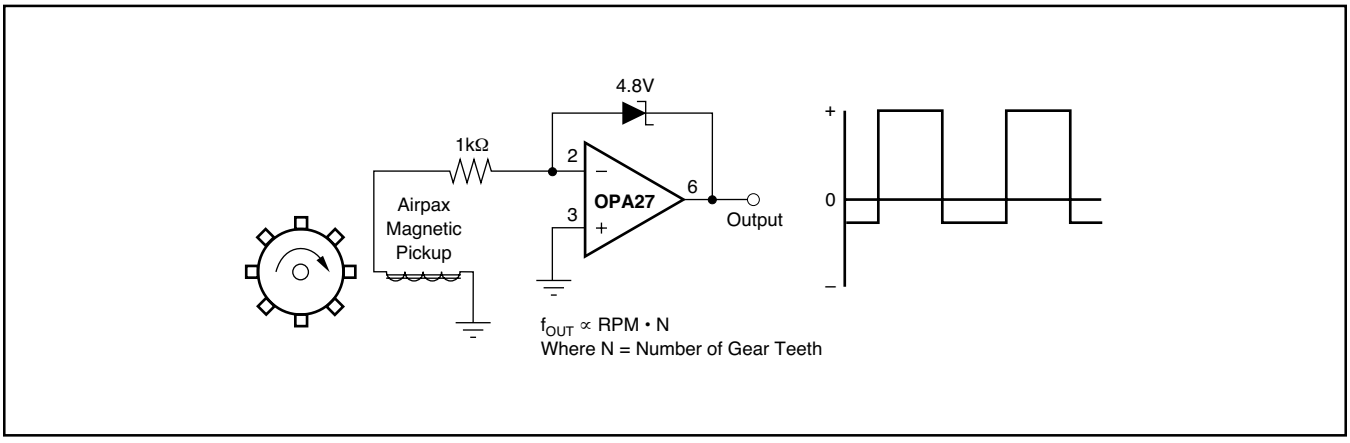


FIGURE 21. Magnetic Tachometer.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA27GP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA27GP	Samples
OPA27GU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	Samples
OPA27GU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	Samples
OPA27GU/2K5E4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	Samples
OPA27GUE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	Samples
OPA27GUG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	Samples
OPA37GP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA37GP	Samples
OPA37GPG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA37GP	Samples
OPA37GU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 37U	Samples
OPA37GU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 37U	Samples
OPA37GUE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 37U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

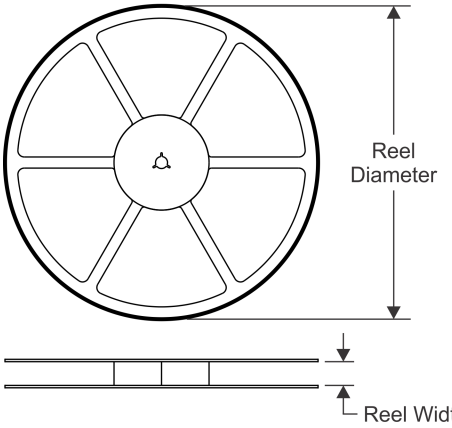
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

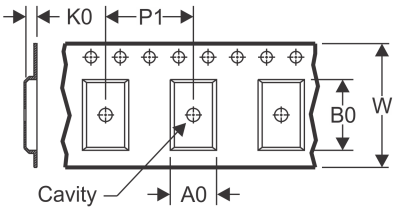
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

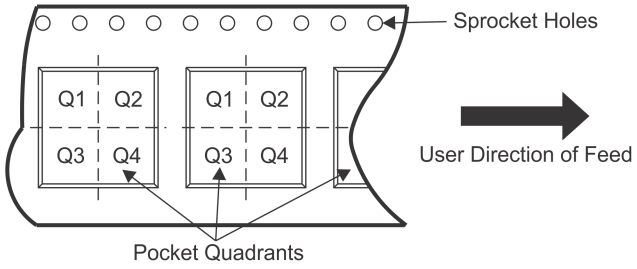


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

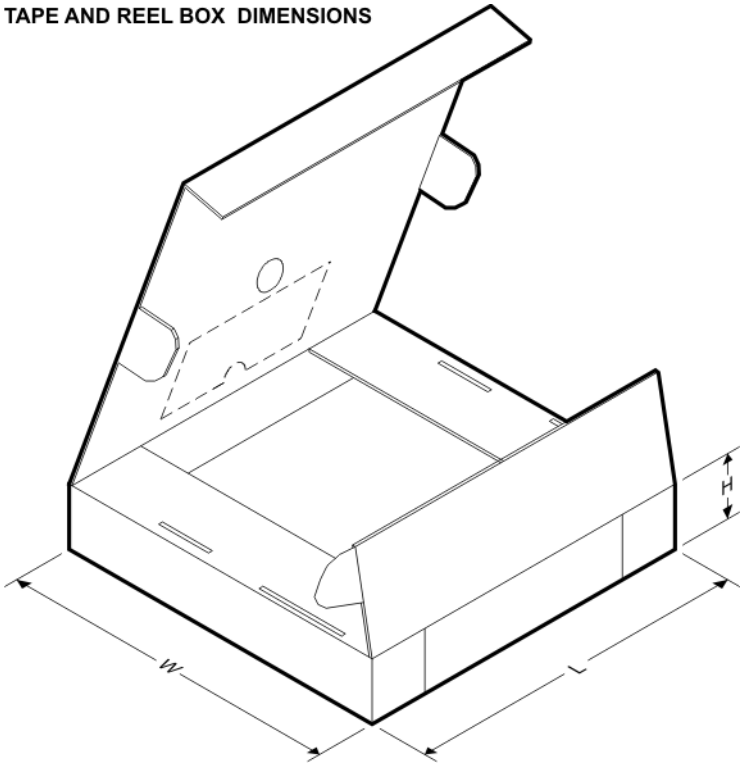
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA27GU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA37GU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

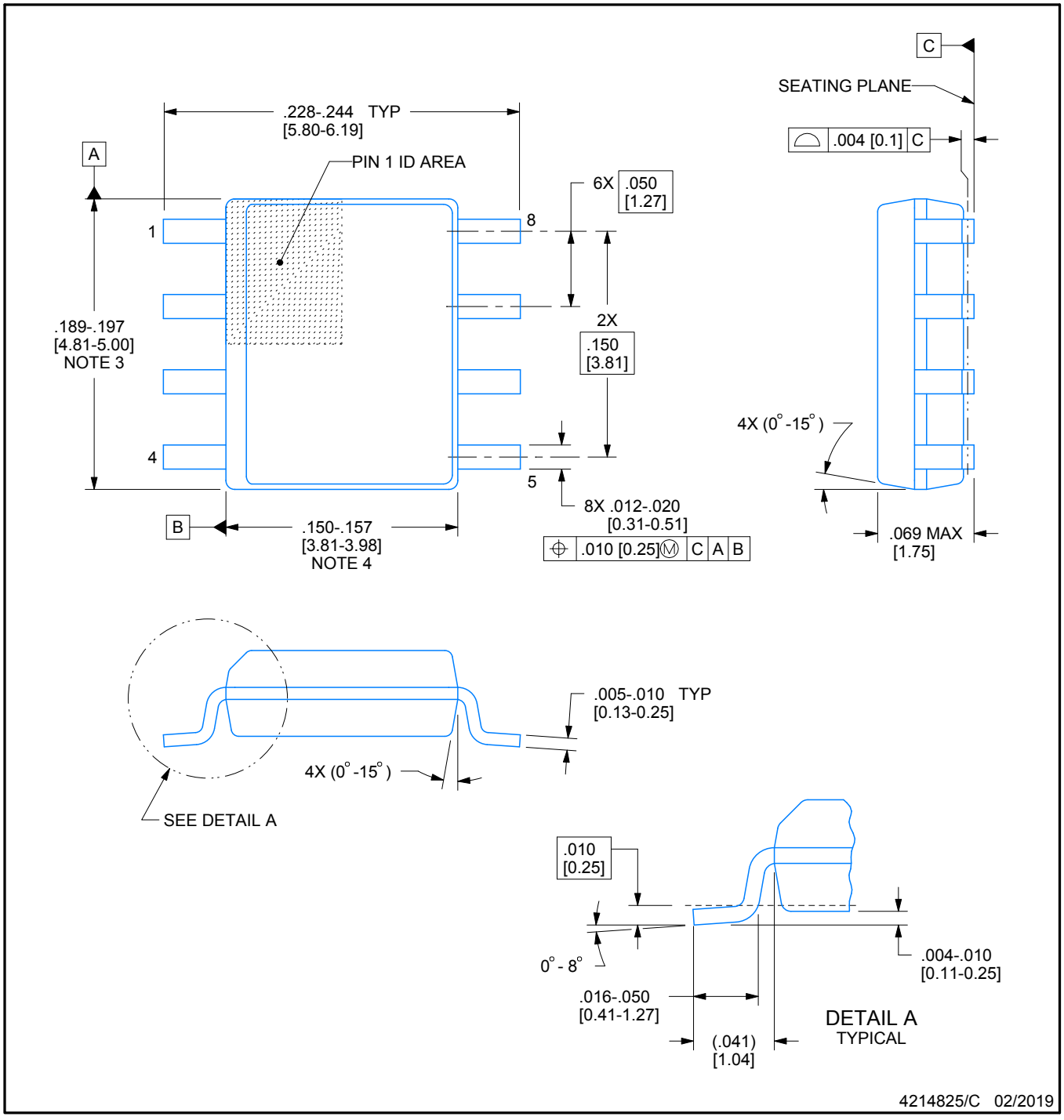
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA27GU/2K5	SOIC	D	8	2500	853.0	449.0	35.0
OPA37GU/2K5	SOIC	D	8	2500	853.0	449.0	35.0

PACKAGE OUTLINE

D0008A

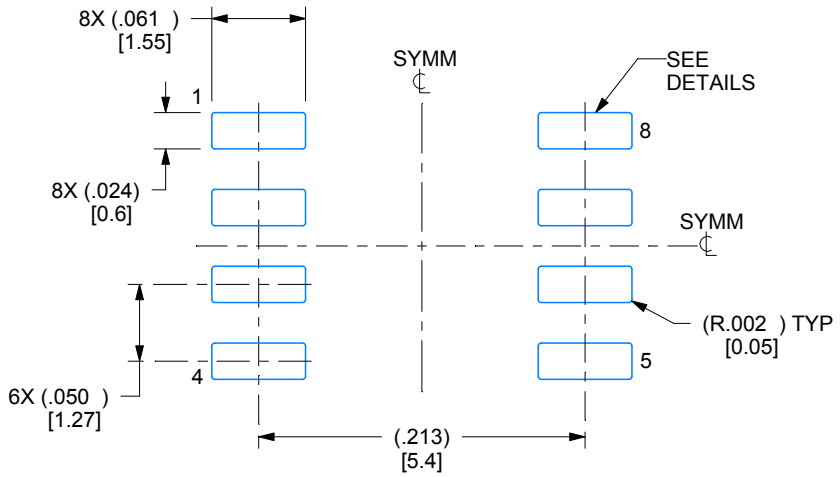
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

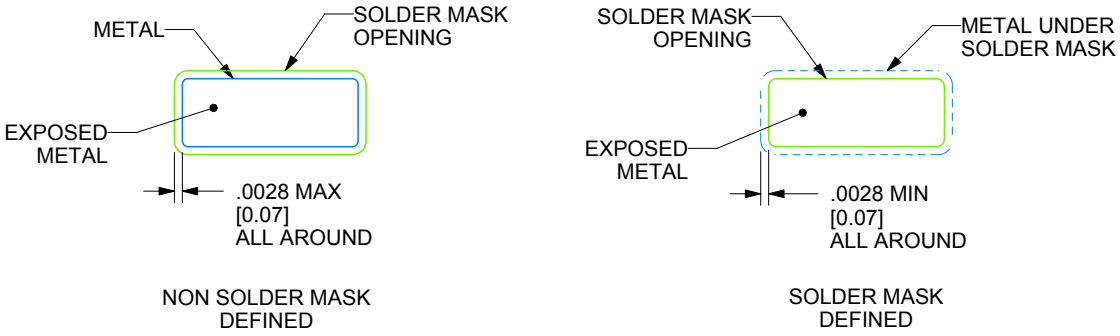


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

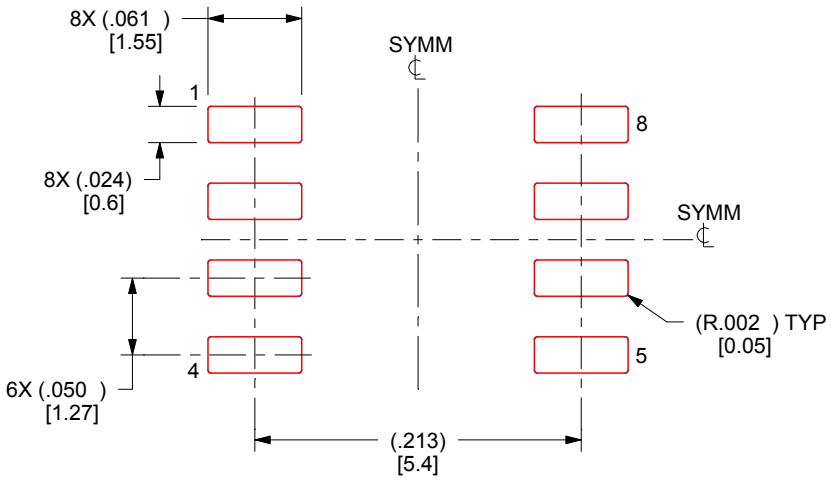


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



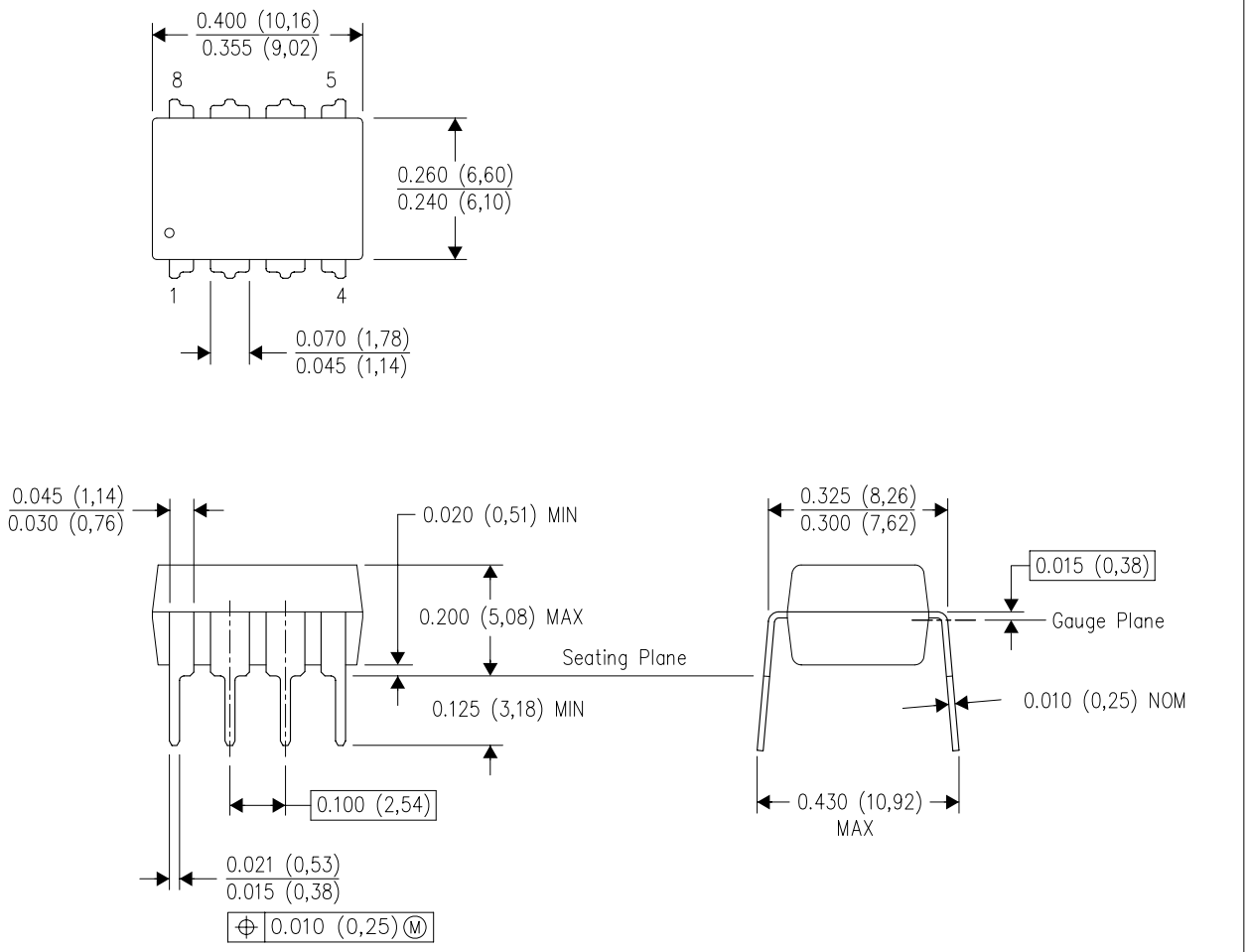
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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