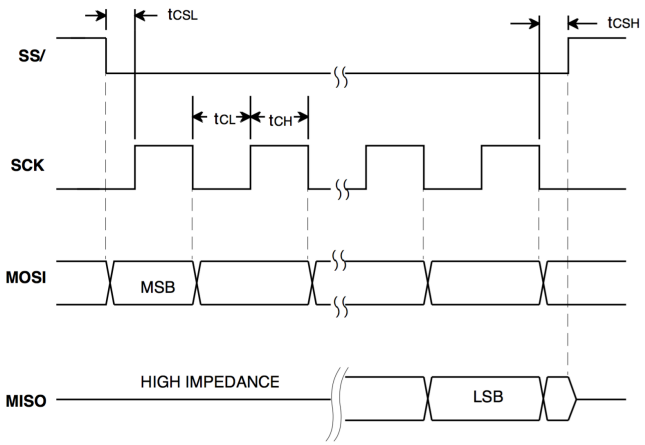
Counter Click - Informations pratiques

Le module counter click permet de décoder les signaux A et B provenant des encodeurs. Il est ensuite possible de récupérer la position de l'arbre à l'aide de l'interface SPI.

Le principal composant du module est le LS7366R. Voici la structure d'un message :



Une fois la communication SPI établie le master (ATmega) peut envoyer des instructions de 8bits pour récupérer ou définir la valeur des différents registres du LS7366R. Voici la structure des instructions envoyées par le Master :

IR. The IR is an 8-bit register that fetches instruction bytes from the received data stream and executes them to perform such functions as setting up the operating mode for the chip (load the MDR) and data transfer among the various registers.

B7	B6	B5	B4	B3	B2	B1	B0

B2 B1 B0 = XXX (Don't care)
B5 B4 B3 = 000: Select none
= 001: Select MDR0
= 010: Select MDR1
= 011: Select DTR
= 100: Select CNTR
= 101: Select OTR
= 110: Select STR
= 111: Select none
B7 B6 = 00: CLR register
= 01: RD register
= 10: WR register
= 11: LOAD register

Le registre CNTR est incrémenté ou décrémenté en fonction des signaux de l'encodeur. Il est possible de lire la valeur du compteur directement (0b00100000) cependant puisque CNTR est souvent modifié il est préférable de charger sa valeur dans OTR (0b11101000) puis de lire la valeur dans OTR (0b01101000). De-même il est possible d'écrire directement dans CNTR (0b10100000) mais pour la même raison on préféra écrire la valeur dans DTR (0b10011000) puis charger celle-ci dans CNTR (0b11100000).

Les registre MDR0 et MDR1 servent à configurer le mode fonctionnement du compteur. Selon la configuration le Master recevra ou enverra 1, 2, 3 ou 4 bytes à la suite des instructions de lecture et d'écriture sur CNTR, OTR et DTR. Les opérations sur les autres registres restent inchangées (1 byte seulement).

MDR0. The MDR0 (Mode Register 0) is an 8-bit read/write register that sets up the operating mode for the LS7366R. The MDR0 is written into by executing the "write-to-MDR0" instruction via the instruction register. Upon power up MDR0 is cleared to zero. The following is a breakdown of the MDR bits:

B7	B6	B5	B4	B3	B2	B1	B0

B1 B0 = 00: non-quadrature count mode. (A = clock, B = direction).
= 01: x1 quadrature count mode (one count per quadrature cycle).
= 10: x2 quadrature count mode (two counts per quadrature cycle).
= 11: x4 quadrature count mode (four counts per quadrature cycle).

B3 B2 = 00: free-running count mode.
= 01: single-cycle count mode (counter disabled with carry or borrow, re-enabled with reset or load).
= 10: range-limit count mode (up and down count-ranges are limited between DTR and zero, respectively; counting freezes at these limits but resumes when direction reverses).
= 11: modulo-n count mode (input count clock frequency is divided by a factor of (n+1), where n = DTR, in both up and down directions).

B5 B4 = 00: disable index.
= 01: configure index as the "load CNTR" input (transfers DTR to CNTR).
= 10: configure index as the "reset CNTR" input (clears CNTR to 0).
= 11: configure index as the "load OTR" input (transfers CNTR to OTR).

B6 = 0: Asynchronous Index
= 1: Synchronous Index (overridden in non-quadrature mode)
B7 = 0: Filter clock division factor = 1
= 1: Filter clock division factor = 2

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