III–V Nanowires on Si Substrate: Selective-Area Growth and Device Applications

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(Invited Paper)

***Abstract*—III–V nanowires (NWs) on Si are promising building blocks for future nanoscale electrical and optical devices on Si platforms. We present position-controlled and orientation-controlled growth of InAs, GaAs, and InGaAs NWs on Si by selective-area growth, and discuss how to control growth directions of III–V NW on Si. Basic studies on III–V/Si interface showing heteroepitaxial growth with misfit dislocations and coherent growth without misfit dislocations are presented. Finally, we demonstrate the integrations of a III–V NW-based vertical surrounding-gate field-effect transistor and light-emitting diodes array on Si. These demonstrations could have broad applications in high-electron-mobility transistors, laser diodes, and photodiodes with a functionality not enabled by conventional NW devices.**

***Index Terms*—Field-effect transistor (FET), III–V on Si, light-emitting diode (LED), metal–organic vapor phase epitaxy (MOVPE), nanowires (NWs), selective-area growth (SAG).**

I. Introduction

RECENT advances in heteroepitaxial techniques, such as vapor–liquid–solid (VLS) [1]–[4] method and selective-area growth (SAG) [5], [6], have enabled us to integrate III–V compound semiconductor (III–V) nanowires (NWs) with Si substrates. These materials integrated on Si have been attracting much attention as building blocks for next-generation electronics and photonics because they can be used as fast channels in vertical nanoarchitectures, steep-slope switches, and vertical NW-based high-electron mobility transistors (HEMTs) on Si wafers. The III–V NWs can be used for optical circuits, replacing Cu-based connections in devices, such as nanometer (nm)-scale light source and detectors, as well as large-scale integration (LSI) chips.

The heteroepitaxy of planar III–V on Si substrates has been challenge since 1980, because mismatches in lattice constants, thermal expansion coefficients, and polar nature cause misfit dislocations, threading dislocations, and antiphase domains (or boundaries) that degrade electrical and optical performance. Although growth techniques, such as two-step growth [7], cycle annealing [8], microchannel epitaxy (MCE) [9], and flow-rate modulation epitaxy (FME) or migration-enhanced epitaxy [10], [11] have not eliminated these defects and dislocations, they have made it possible to make III–V-based light-emitting diodes (LEDs), field-effect transistors (FETs), and APDs on Si because they reduce the number of defects and dislocations as much as possible and enable the active regions of these devices to be separated from defect or dislocation layers by using strain compensation layers or buffer layers.

Since Märtensson's pioneering work on As/P-related III–Vs NWs was reported in 2004 [12], several tens of papers regarding the III–V NW growth on Si substrates have been published [13]–[58]. It should be noted that the growth and applications of nitride-related NWs on Si has been reported by Kishino *et al*. [59]. Almost all reports have focused on the basics of crystal growth of the III–V NWs on Si because we are in only the dawn of III–V NWs/Si integration. So far, the growth of GaAs [12], [14], [16], [22], [23], [25]–[29], [31], [32], [34], [37], [39]–[44], [46], [49]–[51], [53], [55]–[58], InP [13], [15], [16], [18], [20], [33], [35], [41], [44], [52], InAs [16], [21], [24], [26], [30], [38], [44], [45], [47], [48], [54], GaSb [57], and ternary-alloy [18], [21], [39], [40], [43], [57], [58] NWs on Si have been reported, and these NWs were grown by the VLS, catalyst free [21], [24], [29], [34], [38], [40], [45], [52], [55], [57], and SAG methods [43], [48], [54], [58]. The III–V NW-based devices, such as LEDs [39], [58], surrounding-gate FETs integrated on Si with these growth methods have recently been demonstrated [38], [54], and unique photovoltaic devices using III–V NW/Si heterojunctions have also investigated [45].

In the heteroepitaxy of III–V NWs, one must consider not only the conventional problems in III–Vs/Si integration, but also the following four problems: 1) positioning for NWs; 2) polarity in III–V NWs; 3) unintentional doping from the Si substrate; and 4) misfit dislocation at the heterointerface.

1) *Positioning of NWs:* Though positioning is a problem in other nanostructures, lithographic techniques, such as positioning of metal catalysts in VLS or openings in SAG are effective for defining the nucleation sites of NWs.

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2) *Polarity in III–V NWs:* Conventional III–V NWs tend to grow in the ⟨1 1 1⟩B or ⟨1 1 1⟩A directions. For example, InAs NWs preferentially grow in the ⟨1 1 1⟩B direction, so vertically aligned InAs NWs can be grown on a III–V(1 1 1)B substrate. On the III–V(1 1 1)A surface, the InAs NWs grown in three equivalent tilted ⟨1 1 1⟩B directions. The ⟨1 1 1⟩ direction of group-IV semiconductors, on the other hand, do not show different polarities as III–Vs. Thus, in III–V/Si heteroepitaxy equivalent surface orientations and directions always occur on the Si(1 1 1) surface and these equivalencies form antiphase domains in case of III–V/Si heteroepitaxy. Instead of the antiphase-domain formation, equivalent growth directions always occur in case of III–V NW/Si integrations, i.e., on Si(1 1 1) such III–V NWs grow in vertical ⟨1 1 1⟩ and three equivalent tilted ⟨1 1 1⟩ directions at the same time. The differences result either from the coexistence of (1 1 1)A and B surfaces that are formed when Si is etched by a metal catalyst during VLS growth, or from termination of group-III or V atoms on the Si(1 1 1) surface during SAG. For rational design of NW applications taking advantage of geometries, we have to control such equivalent growth directions into vertical ⟨1 1 1⟩ direction.
3) *Unintentional doping from Si substrate:* In the VLS growth of NWs, metal catalysts corrosively etch the Si surface and release Si atoms that can diffuse into the NWs [16], and in catalyst-free growth, Si atoms can easily diffuse into III–V NWs because of high temperatures required for the catalyst-free growth. The unintentional doping from the Si substrate is thought to form a gradual carrier distribution inside III–V NWs. In such case, a highly doped n-type layers always form close to the heterointeface resulting from the unintentional doping, and degrade performance in III–V NW applications. To improve the performance, we have to suppress or control the doping. Effective ways to do that, however, have not been found because there have been few investigations of this kind of doping. Low-temperature (LT) buffer growth could probably suppress the unintentional dopings.
4) *Misfit dislocation at heterointerface:* The heteroepitaxy of lattice-mismatched systems usually introduce misfit dislocation networks at the interface. The lattice mismatches is 4.1% for the GaAs/Si system, 8.1% for the InP/Si system, and 11.6% for the InAs/Si system. Generally, misfit dislocation networks, which Burger's vector of ⟨2 −1 −1⟩ are formed in (1 1 1) plane. Misfit dislocations with a period corresponding to the value calculated from the lattice mismatch are observed in InAs NWs/Si system [30]. These misfit dislocations could probably be avoided by reducing the diameter of the NW, Ertekin *et al*. and Flank have calculated the diameter below which the NW is coherent (without misfit dislocation) and plastic (with misfit dislocations) growth [60], [61]. Coherent growth has recently been shown in experiments with thin GaAs NW/Si interfaces [43]. The effect of these misfit dislocations on NW-based applications on Si has not been investigated. These perceptions regarding dislocations will be important parameters for NW-based devices on Si and new concept using III–V NW/Si heterojunctions [45].

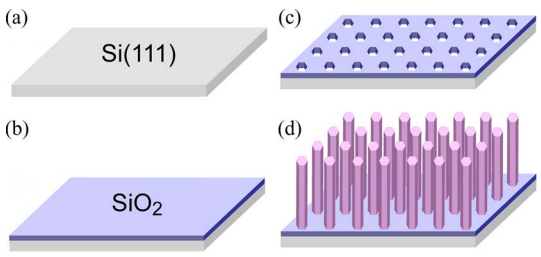

Fig. 1. Illustrations of SA-MOVPE. (a) Surface treatment by RCA cleanings. (b) Deposition of 20-nm-thick SiO_2 film on Si(1 1 1) substrate by thermal oxidation. (c) Definition of hexagonal patterns by EB lithography and wet chemical etching. (d) MOVPE growth.

In this paper, we review the SAG of III–V NWs on Si substrate and report recent progress in this field. We explain key techniques for controlling the growth directions of III–V NWs on Si and also describe the results obtained using transmission electron microscopy (TEM) to investigate the heterointerface of III–V NWs on Si. We focus on InAs NWs, GaAs NWs, and InGaAs NWs because these materials are the good ones to use in electrical and optical devices. Finally, we demonstrate the integration of III–V NW-based surrounding-gate FETs and LEDs on Si substrates.

II. Experiments

This section describes in details investigation of the SAG of III–V NWs on Si and also explains growth parameters for III–V NWs.

A. Selective-Area Metal–Organic Vapor Phase Epitaxy

We used (1 1 1)-oriented Si substrates. We used n-Si(1 1 1), n^+-Si(1 1 1), p-Si(1 1 1), and p^+-Si(1 1 1), but the growth of III–V NWs on Si that will be shown in this paper was typically done on an n-Si(1 1 1) substrate. The processes in selective-area metal–organic vapor phase epitaxy (SA-MOVPE) are shown in Fig. 1. First, the substrates were etched with hydrofluoric (HF) solution and cleaned by RCA cleaning with SC1 and SC2 solutions ($1NH_4OH{:}1H_2O_2{:}5H_2O$ and $1HCl{:}1H_2O_2{:}6H_2O$) at 75 °C to remove metal particles and contamination from their surfaces [see Fig. 1(a)]. Then, 20-nm-thick SiO_2 was formed by using a thermal oxidation process at 950 °C [see Fig. 1(b)]. The formation of SiO_2 at high temperature helps to avoid heat shrink of SiO_2 during SAG of III–V on Si. Electron-beam (EB) lithography and wet chemical etching or reactive-ion etching (RIE) were then used to form periodic opening patterns on the Si surface on which SiO_2 had been formed [see Fig. 1(c)]. The opening diameters d_0 ranged from 15 to 600 nm. The partially masked substrates were then degreased with organic solvents in an ultrasonic bath and slightly etched with buffered HF (BHF) solution for 3 s to remove the native oxide that had formed on the opening area during these processes. Finally, NWs were grown on the mask substrate by MOVPE [see Fig. 1(d)].

B. Growth Conditions for III–V NWs in SA-MOVPE

The NW growth was performed using a low-pressure (0.1 atm) horizontal-reactor MOVPE system. The carrier gas used in this growth was pure hydrogen (H_2) that had been purified by passing it through Pd films. The total flow rate of the gases was maintained at 5.75 standard liters per minute (SLM). The group-III-atom precursors used in this study were trimethylgallium (TMGa), trimethylindium (TMIn), and trimetylaluminium (TMAl), and the group-V-atom precursor was 5% arsine (AsH_3) in H_2. Silane (SiH_4) gas was used for n-type doping, and diethylzinc (DEZn) was used for p-type doping. Prior to growth, thermal cleaning in an H_2 ambient was carried out at 925 °C to remove the native oxide that had formed on the opening areas of the masked substrates when transferring the samples into the reactor. Native oxide about 1 nm thick formed on the opened patterns.

Optimum SA-MOVPE growth conditions for conventional III–V NWs themselves in SA-MOVPE have been reported elsewhere [62]–[68]. GaAs NWs were grown for 60 min at 750 °C, while the partial pressures of TMGa ([TMGa]) and AsH_3 ([AsH_3]) were 1.0×10^{-6} and 2.5×10^{-4} atm, respectively. InAs NWs were grown for 20 min at 540 °C, while the partial pressures of TMIn ([TMIn]) and [AsH_3] were 4.7×10^{-7} and 1.3×10^{-4} atm, respectively. InGaAs NWs were grown for 30 min at 670 °C, while [TMGa], [TMIn], and [AsH_3] were 5.9×10^{-7}, 9.2×10^{-7}, and 1.3×10^{-4} atm, respectively. The ratio of [TMIn] to [TMGa] + [TMIn] was about 0.62.

C. Characterization of III–V NWs

High-resolution TEM images of samples that had been sliced into thin sections by using a focused-ion-beam (FIB) and Ar-ion-miling techniques were acquired using a TEM (HITACHI H-9000UHR). The acceleration voltage was 300 kV, and the EB was incident along the $\langle -1\,1\,0 \rangle$ direction. Real image calculated from TEM images by deriving a series of $\langle -1\,1\,1 \rangle$ reciprocal lattice spots from fast Fourier transform (FFT) patterns of a high-resolution TEM image, and then, using an inverse FFT to transform those patterns into real images in which only the (1 1 1)A planes that in the $\langle -1\,-1\,2 \rangle$ direction were approximately 3.32 Å apart.

Raman scattering measurements were used to investigate strains in the III–V NWs grown on Si. An He–Ne laser, whose wavelength was 632.8 nm, was focused on an approximately 2-μm spot on the substrates with the NWs grown on them. The laser power was about 0.1 mW. The incident direction of the excitation light was along the $\langle 1\,1\,1 \rangle$B direction in (1 1 1) backscattering geometry. Microphotoluminescence (μ-PL) was carried out at 4.2 K. The excitation light was an He–Ne laser, which was focused on an approximately 2-μm spot on the substrate, and about 10 NWs were included in the spot.

III. SA-MOVPE Growth of III–V NWs on Si

This section discusses the SA-MOVPE growth of III–V NWs on Si(1 1 1) substrates also describes a key process for controlling the growth directions of the III–V NWs. III–V NWs tend to grow in $\langle 1\,1\,1 \rangle$B direction or, for InP NW, $\langle 1\,1\,1 \rangle$A direction. In III–V compound semiconductors, the notation B means that the outermost atomic layers are group-V atoms and the notation of A means that the outermost atomic layer are group-III atoms. Fig. 2(a) and (b) shows typical results of SA-MOVPE growth of InAs NWs on InAs(1 1 1)B and (1 1 1)A surfaces. On the (1 1 1)B substrate, the NWs grew normal to the substrate, while on the (1 1 1)A substrate the NWs grew in three equivalent $\langle 1\,1\,1 \rangle$ directions 19.6° tiled from the (1 1 1)A surface. On Si(1 1 1) surface, these vertical and tilted NWs grow at the same time, as shown in Fig. 2(c). This is because the Si(1 1 1) surface has both (1 1 1)A and (1 1 1)B surfaces.

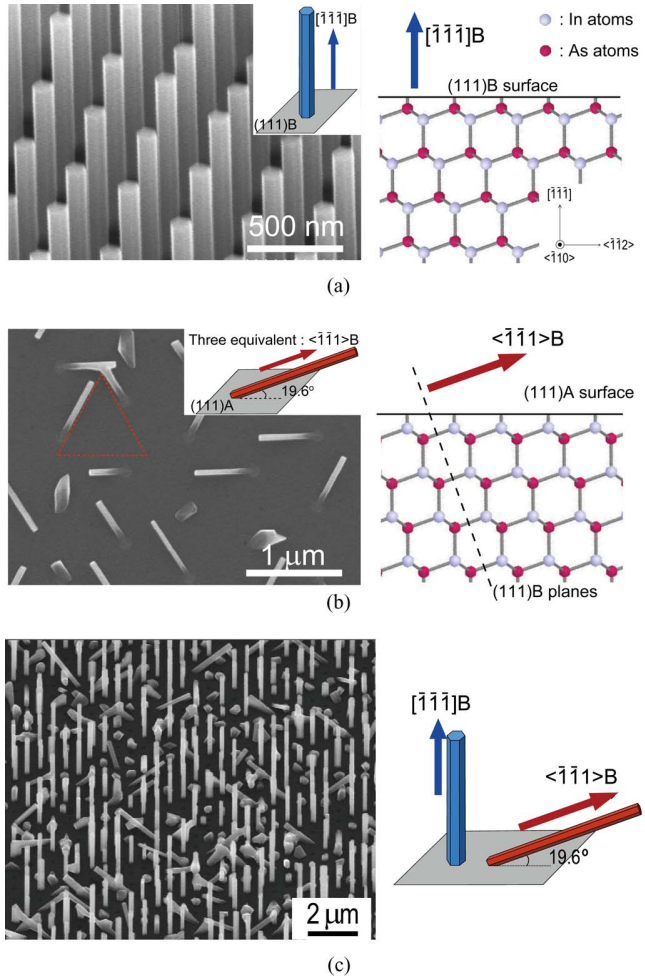

Fig. 2. (a) SEM image of InAs NW growth on InAs(1 1 1)B and schematics for InAs(1 1 1)B structure. Blue-colored arrow shows growth direction of the InAs NWs. (b) Plan view of SEM image of InAs NW growth on InAs(1 1 1)A and schematics of InAs(1 1 1)A structure. Red-colored arrow shows growth direction of the InAs NWs. (c) Typical growth results of InAs NW on Si.

A. Control of Growth Directions for III–V NWs on Si

The SA-MOVPE initiates from atomically flat surface without any catalyst. The coexistence of vertical and tilted NWs, as shown on Fig. 2(c), was caused from a formation of four types of chemical structures in Fig. 3(a)–(d). These structures are results of the Si terminated or incorporated by group-III and

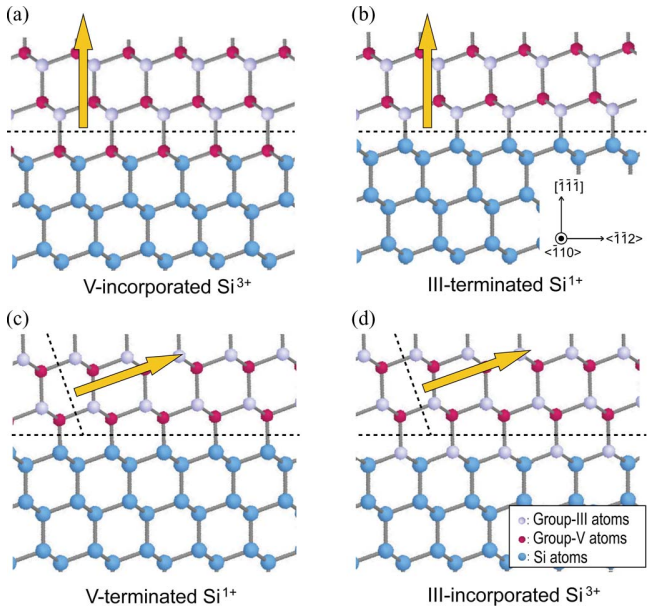

Fig. 3. Illustrations of chemical structures. (a) Group V incorporating Si^{3+} structure. (b) Group III terminated Si^{1+} surface. (c) Group V terminated Si^{1+} surface. (d) Group III incorporating Si^{3+} structure. These are viewed from $\langle -1\ 1\ 0\rangle$ direction. Yellow arrows indicate III–V NW-growth direction. Adopted from [36] (American Chemical Society, copyright 2008).

group-V atoms. Thus, the growth directions of the III–V NWs can be controlled by optimizing the initial surface and growth conditions. Vertical growth can be obtained by simply forming an (1 1 1)B-oriented surface on the Si(1 1 1) surface. Si(1 1 1) surface usually has Si^{1+}, Si^{2+}, and Si^{3+} structures between Si and native oxide (SiO_2) [69], [70]. As shown in Fig. 3(a) and (b), once As-incorporating Si^{3+} and/or In-terminated Si^{1+} has formed on the Si surface, only vertical III–V NWs should grow on the Si(1 1 1) substrates. For precise control of the NW-growth directions in SA-MOVPE, surface reconstructions and the removal of native oxide should be considered.

Various kinds of reconstructed Si(1 1 1) surfaces have been obtained under in case of ultrahigh-vacuum (UHV) condition studies, metastable reconstructed $n \times n$ ($n = 1, \sqrt{13}, 2$) and c2 $\times$ 4 surfaces at temperatures from 500 to 830 °C and 1 $\times$ 1 reconstructed structure at above 830 °C. We should note that the growth temperature windows for most III–V semiconductors are within the range in which metastable reconstructions form. Such metastable surface reconstructions are thought to randomize the orientation of dangling bonds and/or to disrupt the uniform nucleation of III–V growth on the Si surface. A promising way to avoid the formation of metastable surface reconstructions is to cool the Si(1 1 1) surface to 400 °C in a H_2 ambient, because the 1 $\times$ 1 reconstructed surface that was formed at a higher temperature can regenerate at 400 °C, and also, group-V atoms should be replaced with the outermost Si atoms of 1 $\times$ 1 reconstructed surface because it is equivalent to a V-atoms-terminated Si^{3+} surface and a (1 1 1)B-oriented surface. Conveniently, the Si(1 1 1):As 1 $\times$ 1 reconstructed surface found to be formed at temperature below 430 °C in an As ambient [71].

Native oxide disrupt the nucleation process of III–Vs, and *in situ* thermal cleaning at above 900 °C is effective for removing the native oxide and forming the Si(1 1 1) 1 $\times$ 1 reconstructed surface. The thermal cleaning at high temperature is common process for cleaning Si(1 1 1) to control the growth directions of III–V NWs on Si(1 1 1) by SA-MOVPE. These processes strongly depend on bonding strength between group-III atoms and Si atoms. Next, we describe typical growth results of InAs NWs on Si(1 1 1) substrate.

B. Control of Growth Directions for InAs NWs on Si

InAs is a narrow-bandgap semiconductor and has high-electron-mobility (at room temperature (RT), 20 times higher than that of Si) because of its small electron effective mass. Because InAs has Fermi level pinning at conduction band, this material is less effective against surface depletion resulted from surface states. This means that conductive InAs NWs can easily be obtained without using any surface passivations. Although, the crystal lattice mismatch between InAs and Si is very large (11.6%), the VLS method can be used to grow InAs NWs on Si. It is, however, difficult to control the growth direction of InAs NWs because of the polar/nonpolar nature of these materials. Thus, this material is useful in studies investigating the way to control the growth directions of III–V NWs on Si(1 1 1).

We, therefore, studied the relation between the growth yields of InAs NWs and the AsH_3 supply conditions prior to the growth. In these studies, we used thermal cleaning at above 925 °C for 5 min prior to the growth in order to remove native oxide from the opening area of patterns. The openings were 60 nm in diameter and the partial pressure of AsH_3 prior to the growth was 2.5×10^{-4} atm. Fig. 4 shows a series of growth sequences in which for each sequence we evaluated the percentage of vertical NWs, tilted NWs, and no growth. We confirmed the reproducibility of each percentage with 30 wafers: the standard deviation was within $\pm$ 1%.

With the conventional sequence shown in Fig. 4(a), the yield of vertical InAs NWs is approximately 31% and that of tilted NW is 17%, and as shown in Fig. 5, no growth yield obtained with that sequence could be as high as 52%. The result suggests that with the conventional sequence, the formation of (1 1 1)B-oriented surface is insufficient because of thermal desorption of In atoms from the Si substrate and Si(1 1 1) surface reconstruction. The MOVPE system uses pure H_2 as the carrier gas, but no hydrogen terminates on Si surface because the Si–H bond is thermally weak at 540–925 °C. A complex As atom termination of the reconstructed Si(1 1 1) surface occurred prior to the growth, and this complex surface reconstruction blocked the SAG. Furthermore, In atoms required for making a (1 1 1)B-oriented surface on Si(1 1 1) can easily be desorbed from Si surface at a high temperature. Although, the complex surface is assumed to be formed in the sequence shown in Fig. 4(a), the yield of the vertical InAs NWs is small (31%). Fig. 5 shows [AsH_3] dependency of NW growth yields during cooling after thermal cleaning in Fig. 4(a). In this result, the vertical NW growth yield was 70% when the [AsH_3] was zero. The percentage of no growth was increased with the increment of [AsH_3].

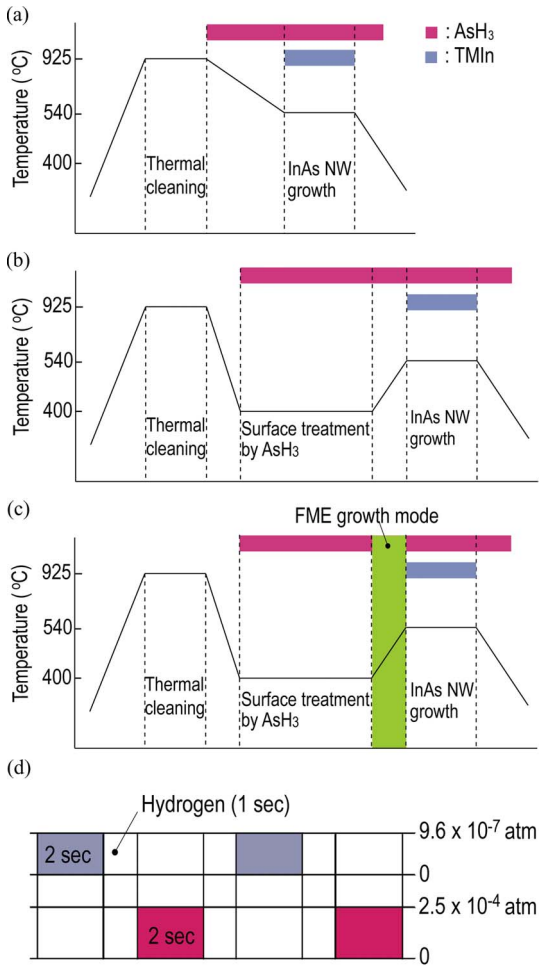

Fig. 4. (a)–(c) Schematic illustrations of gas flow and temperature sequence for InAs NW growth on Si. (d) Schematic diagram of flow-rate modulation mode. Adopted from [36] (American Chemical Society, copyright 2008).

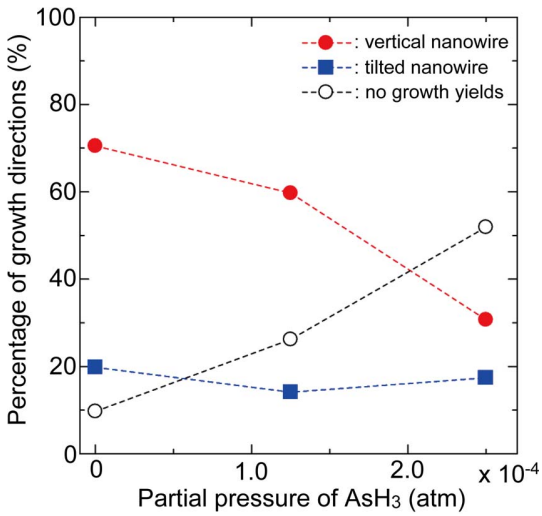

Fig. 5. Percentage of growth results with a growth sequence of Fig. 4(a) as a function of partial pressure of AsH_3.

This means that formation of As-incorporated or reconstructed Si surface was increased with the increment of [AsH_3]. These reconstruction and incorporation of Si surfaces blocked the nucleation process. Such surface reconstructions and In atom desorption should, therefore, be controlled to ensure the formation of (1 1 1)B-oriented Si(1 1 1) surface.

Cooling the Si(1 1 1) surface to 400 °C in H_2 ambient prevents formation of the reconstruction and incorporation of Si surface, because the 1×1 reconstructed surface that formed at a high temperature can regenerate at 400 °C. We, therefore, tried to change the Si(1 1 1) 1×1 surface to a Si(1 1 1):As 1×1 reconstructed surface by treating it with AsH_3 at 400 °C, as shown in Fig. 4(b). This sequence increased the vertical NW-growth yield to 67%, decreased the yield of 19.6°-tilted InAs NW to 11%, and had little effect on the no growth yield 22%, the small percentage of the 19.6°-tilted InAs NWs indicates that the formation of In-terminated Si^{1+} or As-incorporating Si^{3+} surface, which are crystallographic equivalent to a (1 1 1)B-oriented surface, was still insufficient. This is because that As adatoms were desorbed from the Si surface during the substrate temperature set to the growth temperature [see Fig. 4(b)]. The percentage of the vertical NW, tilted NW, and no growth were almost same with the variation of [AsH_3] during the treatment of AsH_3 at 400 °C shown in Fig. 4(b). This behavior can be attributed to the decomposition or desorption of As adatoms from the Si surface being the dominant process as the substrate temperature was rising to the growth temperature. The tilted-NW growth yields were caused from the formation of (1 1 1)A surface after the desorption process. In this case, formation of In-incorporated Si^{3+} surface was thought to be dominant for the tilted-NW growth. We, therefore, think that the control of desorption or decomposition of V atoms process is important for suppressing the growth of tilted NWs.

Consequently, we used the growth sequence shown in Fig. 4(c) and (d) to avoid decomposition and desorption of As atoms. First, the substrate was cooled down to 400 °C after thermal cleaning. Next, AsH_3 was supplied at this temperature to form the As-incorporating Si^{3+} surface shown in Fig. 3(a). Because As and In atoms should be efficiently supplied to the Si(1 1 1) surface in order to form a (1 1 1)B-oriented surface just before InAs NW growth, we used the FME at 400 °C [10]. FME is a method of alternating supplying group-III or group-V precursor supply during MOVPE. The purpose of the FME is to enhance the termination of As-incorporating Si^{3+} by In atoms, and termination of bare Si^{1+} surfaces by In atoms because the termination of Si^{1+} surface by group-III atoms also forms (1 1 1)B-like surface. We also used a brief pulse of H_2 between the TMIn and AsH_3 supply to enhance the exchanges of supplied materials. Fig. 4(d) outlines the optimum gas-flow sequence of the FME. The FME mode was carried out for 20 cycles at 400 °C, after which typical InAs NW growth was carried out at 540 °C. As a result, 99% of all the NWs were vertical direction, and 1% were tilted NWs, and no-growth yield was zero, as shown in Fig. 6. These results suggest that this growth sequence sufficiently formed (1 1 1)B-oriented on Si(1 1 1).

The complete vertical-aligned InAs NWs on Si(1 1 1) obtained under optimized conditions are shown in Fig. 7(a) and

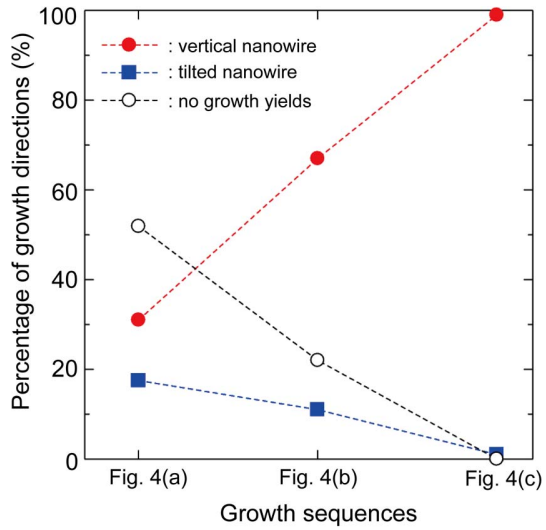

Fig. 6. Percentage of growth results in each growth sequence.

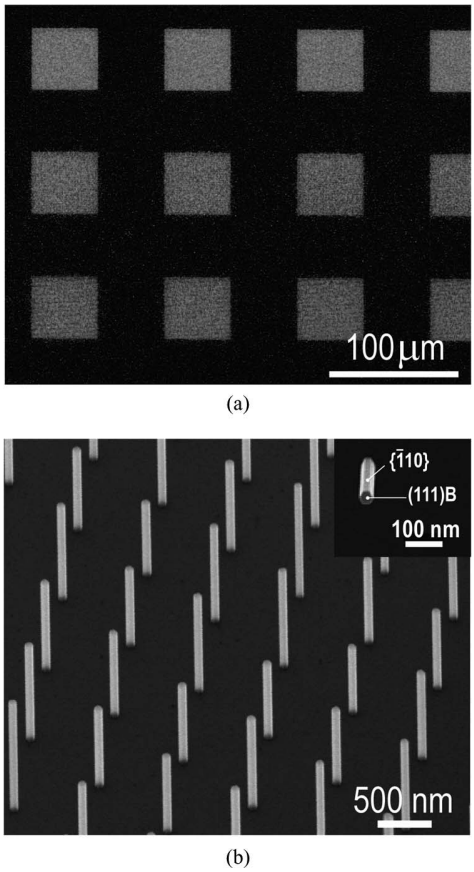

Fig. 7. (a) Overview of InAs NW arrays on patterned substrate and (b) 45°-tilted view of SEM showing vertical InAs NW array. Inset shows a plan view of a InAs NW. Side facets are $\{-1\,1\,0\}$ planes and hexagonal-shaped cross section is (1 1 1)B plane.

(b). Fig. 7(a) exhibits an overview of InAs NW arrays on Si(1 1 1) substrate. The position-controlled InAs NWs, shown in Fig. 7(b), were formed within the gray square prepatterned

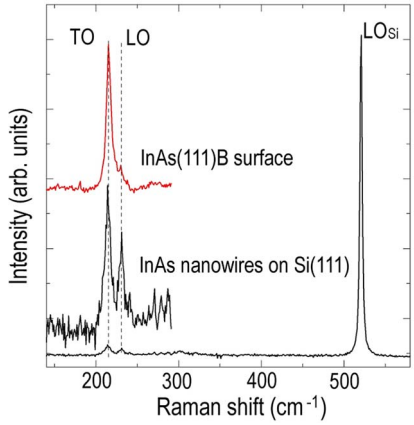

Fig. 8. Raman spectra of grown InAs NWs (black solid line) and InAs(1 1 1)B substrate (red solid line). Adopted from [36] (American Chemical Society, copyright 2008).

regions (each $50 \times 50\ \mu m^2$) in Fig. 7(a). Between the prepatterned regions, hillocks due to lattice mismatch and unexpected InAs NWs [45] were formed. The prepatterned regions were readily fabricated by using EB lithography and wet chemical etching. Here, we used the patterns, whose opening diameter was 70 nm and whose pitch ranged from 400 to 800 nm. The InAs NWs grew only in the openings and oriented perpendicular to the surface. They were an average of 70 nm in diameter and average of 2 μm in height. Size fluctuation of NW diameters was $\pm$ 4 nm as standard deviation. Fluctuation of height of the InAs NWs, in Fig. 7(b), was thought to be resulted from a variability of nucleation process at the initial stage of the NW growth. Inset of Fig. 7(b) shows a plan view of SEM image. All the NWs had a hexagonal-shaped cross sections with surrounding $\{-1\,1\,0\}$ side facets.

Raman scattering spectra of these NWs on Si and a reference InAs(1 1 1)B substrate are shown in Fig. 8. TO and LO phonon spectra from the NWs and a strong Si LO phonon were observed. The TO and LO phonon spectra have no peakshift as compared to those of the bulk InAs(1 1 1)B surface. This means that the strains generated from the lattice mismatch accommodate only at the interface. The FME mode at low-growth temperature thus seems to have accommodated the strains at the InAs/Si interface. The detailed investigation of heterointerface at InAs NW/Si will be described later.

C. Growth of Vertical-Aligned GaAs NWs

GaAs is widely used to make LEDs, laser (LDs), and photodiodes (PDs) with GaAs-related alloys. Once we can directly fabricate GaAs NWs on Si, we can integrate such devices into the NWs on Si.

The circumstances of GaAs NW growth on Si in SA-MOVPE differ from those of InAs NWs because the growth temperature is higher for GaAs NWs. Ga atoms forming (1 1 1)B orientations via termination to Si^{1+} are easily desorbed from Si surface at high temperatures needed for GaAs growth. The FME mode was not effective for forming vertical GaAs NWs because of this desorption process. Using the FME mode at 400 °C reduced the rate

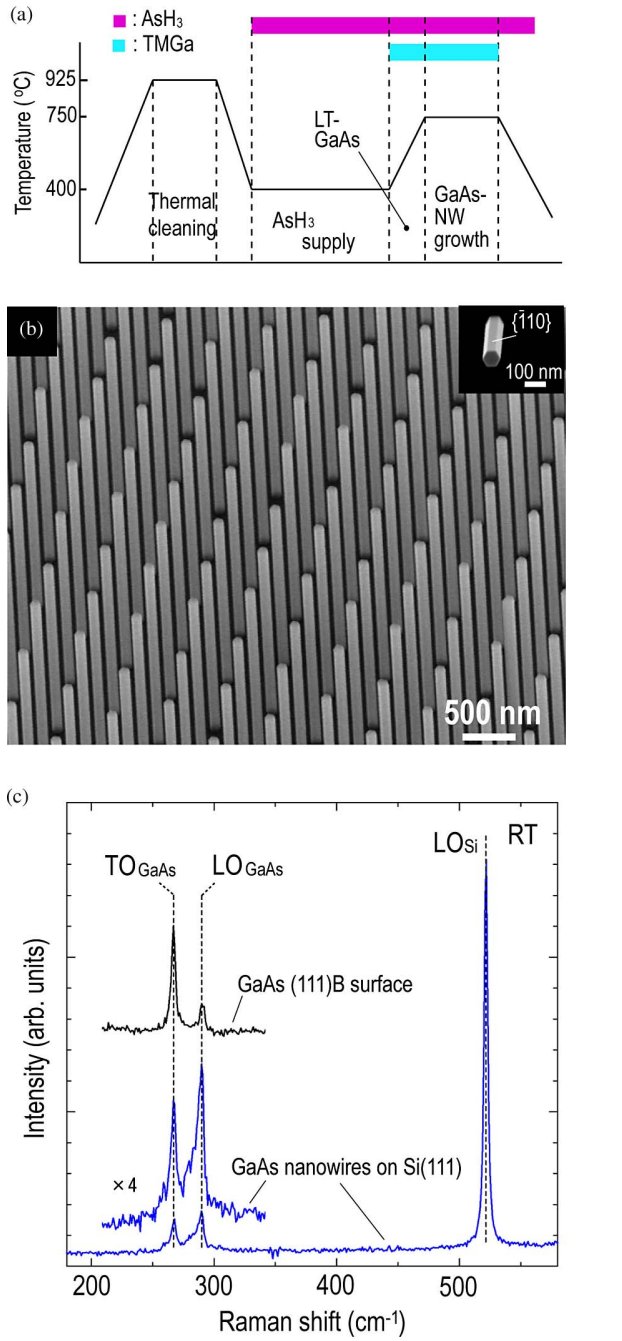

Fig. 9. (a) Growth sequence for GaAs NWs grown on Si(1 1 1) substrate. LT means low temperature and (b) 45°-tilted view of SEM showing NW array on Si(1 1 1) surface. Inset shows a plan view of a GaAs NW. (c) Micro-Raman spectra of GaAs NWs measured at RT. Adopted from [43] (Institute of Physics, copyright 2008).

of GaAs NW growth almost to zero and no-growth yield became approximately 100% because the thermal desorption of Ga and As atoms and formation of metastable surface reconstructions prevented nucleation.

The growth sequence for making vertical-aligned GaAs NWs on Si is illustrated in Fig. 9(a). In this case, surface treatment by AsH_3 at 400 °C for making Si(1 1 1):As 1×1 reconstructed surface is same as that of InAs NW growth on Si. After the treatment of AsH_3, next, a thin GaAs LT buffer layer was grown during temperature changes from 400 to 750°C. This sequence took 3 min, and the expected thickness of the LT buffer layer was about 5 nm. This LT growth is important to prevent the thermal desorption of Ga and As atoms from the Si surface because the As–Si and Ga–Si bonding strength is weak at high temperature.

Following all these steps, GaAs NWs could be grown in the vertical [1 1 1] direction on Si, as shown in Fig. 9(b). The yield of the vertically aligned GaAs NWs was 100% The GaAs NWs in Fig. 9(b) measured 70 nm in diameter and 2.6 μm in height. The standard deviation in diameter fluctuations was $\pm$ 3 nm in this case. The NW diameters were almost equal to that of the mask openings (d_0), which means lateral over growth in the $\langle -1\,1\,0 \rangle$ directions was completely suppressed because of As desorption on the $\{-1\,1\,0\}$ sidewalls. Fig. 9(c) shows the Raman spectra for GaAs NWs. LO and TO phonon peaks can be observed as well as Si LO phonon peak. Neither LO or TO phonons indicate peak shift to that of GaAs bulk. This means that the grown NWs on Si are pure GaAs without strains resulting from large lattice mismatch.

D. Growth of Vertical InGaAs NWs

InGaAs NWs are widely used for expanding the range of functionalities in III–V NWs because of their bandgap engineerings with variation of In/Ga ratio and the combinations. This ternary NW can be used for various applications as electronics and photonics. For example, In-rich InGaAs NWs are expected to become building blocks for NW-based HEMTs and APDs with vertical architectures, and Ga-rich InGaAs NWs are expected to be used in tandem-type solar cells.

The growth conditions for vertically aligned InGaAs NWs on Si(1 1 1) are slightly different from those for vertically aligned InAs NW and GaAs NW on Si. The optimum growth sequence for vertical InGaAs NWs on Si is shown in Fig. 10(a). In this case, the treatment of AsH_3 at 400 °C like GaAs NW and InAs NW was not necessary. Instead, combination treatment of AsH_3 and FME mode at 670 °C became important for making vertical InGaAs NWs on Si. The growth result by using the growth sequence is shown in Fig. 10(b). The percentage of the vertical NW yields was 100%. Other growth sequence, such as for InAs and GaAs NWs on Si yielded tilted NWs and giant hillocks on the masked substrate. This was because the thermal desorption of group-III atoms and intermixing of Ga/In alloys with Si. The Ga–In alloy and Si was thought to enhance the thermal reactions and lead desorption. After the desorption, other (1 1 1)A surfaces were formed. A (1 1 1)B surface orientation due to the incorporation of group-III atoms and Si^{1+} surface were thought to be formed under the sequence illustrated in Fig. 10(a). Detailed investigations will be reported elsewhere.

IV. Investigation of III–V NW/Si Heterointerface

Conventional III–Vs planar on Si have lattice mismatch that usually forms misfit dislocations due to critical thickness with considering isotropic elasticity by Matthews and Blakeslee [72] In case of III–V NWs, these dislocations would be avoided by the nm-scaled footprints. Several calculations have predicted

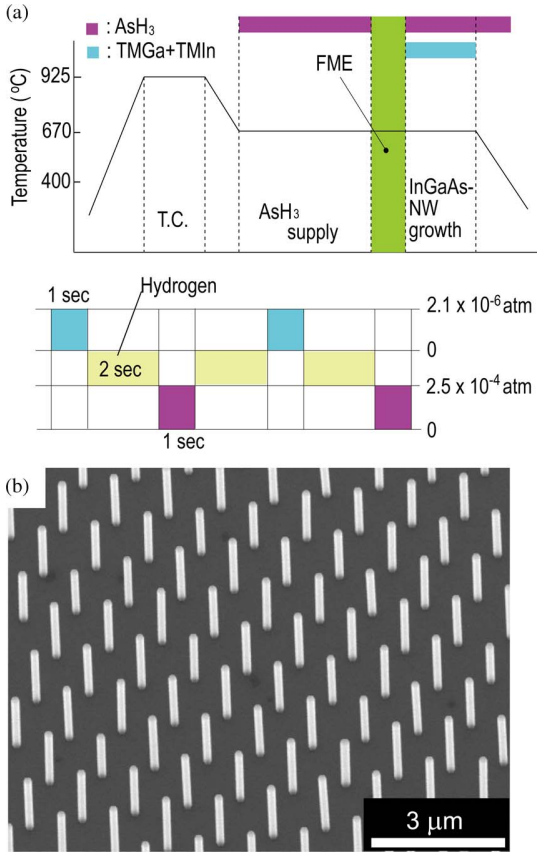

Fig. 10. (a) Schematic illustrations of gas flow and temperature sequence for InGaAs NW growth on Si and schematic diagram of flow-rate modulation mode and (b) 30°-tilted view of SEM showing vertical InGaAs NW on Si.

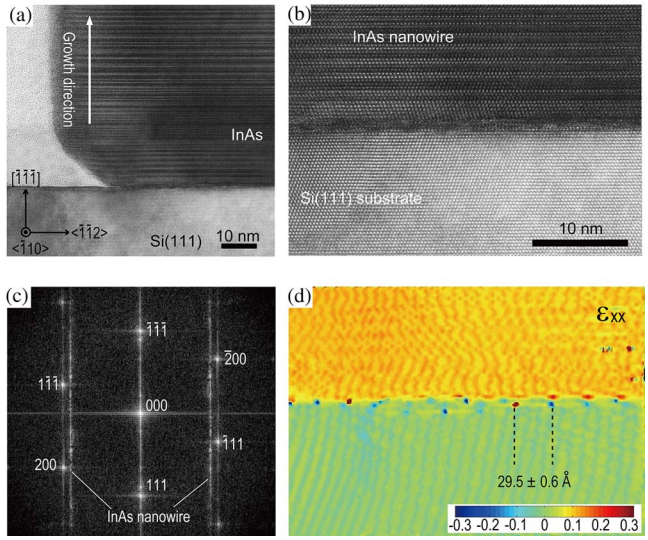

Fig. 11. (a) TEM image of InAs NW on Si(1 1 1) substrate. Incident direction of EB is in $\langle -1\,1\,0\rangle$ direction. (b) High-magnification image of (a). (c) FFT image calculated from (b). Both Bragg spots of Si substrate and InAs NW can be seen in image. (d) ε_{xx} strain mapping estimated from filtered image of (b). Adopted from [36] (American Chemical Society, copyright 2008).

the existence of critical radii below which coherent growth. In SAG, the critical radii are determined by the diameter of nm-scaled openings. This section will show the results of direct observation of heterointerface of III–V NWs on Si, and we will show the coherent growth for GaAs NW on Si.

Fig. 11(a) is a magnified image of TEM for InAs NW on Si. The atomic layer stacking of the InAs were twinned across the heterointerface. Moreover, lamellar dark contrasts, whose thickness is 5 monolayers (MLs) can be observed at the interface. We first filtered the image by using Bragg-spot filtering because the dark contrast due to strain and the twinning at the interface blurred the characterization of the interface. The FFT image is shown in Fig. 11(c). Bragg spots can be seen in Fig. 11(c) addition to those of Si substrate. We next calculated the displacements in the bright spots on the Bragg-spot filtered image into a strain map by using a peak-pair finding technique [73]. Strain mapping estimated from displacement of bright spots in the TEM image is shown in Fig. 11(d). Here, the strains ε_{xx} and ε_{yy} were calculated from the displacement of bright spots in Fig. 11(c) by using a peak-pair finding algorithm [73] and the displacements of the bright spots are defined by $u_{xx} = \Delta x - a_{\mathrm{Si}(x)}$ for the in-plane $\langle 2\,{-}1\,{-}1\rangle$ direction and $u_{yy} = \Delta y - a_{\mathrm{Si}(y)}$ for the vertical $\langle 1\,1\,1\rangle$ direction. The Δx and Δy are the displacements of the bright spots for each direction. The $a_{\mathrm{Si}(x)}$ and $a_{\mathrm{Si}(y)}$ corresponds to the lattice constants in the in-plane and vertical directions of the Si substrate estimated from the TEM image. Also, strain ε_{xx} and ε_{yy} are determined by $\varepsilon_{xx} = \partial u/\partial x$ and $\varepsilon_{yy} = \partial u/\partial y$, where u is $\sqrt{u_{xx}^2 + u_{yy}^2}$. Note that, since the displacement of the atoms is calculated based on the position of the atoms in crystalline Si, unstrained III–Vs are mapped into a layer with a strain in definition.

Fig. 11(d) describes ε_{xx} strain fields, whose x vector is in the $\langle -1\,{-}1\,2\rangle$ directions. Periodical strains along the $\langle -1\,{-}1\,2\rangle$ directions are observed at the interface. The average periodic strain measured from Fig. 11(d) is 29.5 ± 0.6 Å. The Burgers vector due to misfit dislocations on the (1 1 1) plane is in the $\langle -1\,{-}1\,2\rangle$ directions, and the period of the misfit dislocations calculated from the lattice mismatch (11.6%) is 28.8 Å. Similar strain fields due to dislocations were calculated by Ertekin *et al.* [60]. Thus, the periodical strains in Fig. 11(d) are originated from misfit dislocations. We presumed that coherent growth without such dislocations occur in the lattice-mismatched systems when the opening diameters become smaller than that of Fig. 11(d). The critical radii for the coherent growth of InAs NWs on Si were not predicted, but it assumed to be much smaller diameter according from the calculation by Glas [61]. Further investigation is required to control the dislocations at InAs NW/Si interface.

Fig. 12(a) depicts TEM image of heterointerface of a GaAs NW and Si substrate. The diameter at the heterointerface was 103 nm. At first, the GaAs NW was epitaxially grown on Si surface, and rotational twins were observed inside the GaAs NW. Fig. 12(b) shows the magnified TEM image of the GaAs NW/Si interface. After the strain calculation from the image, ε_{xx} and ε_{xy} was shown in Fig. 12(c). From these strain maps, periodical local strains were observed at the interface. The average period for the local strains were 79.9 ± 1.6 Å. Since the calculated periods for misfit dislocation from lattice mismatch in the GaAs/Si system (4.1%) was 84.8 ± 5 Å, these local strains

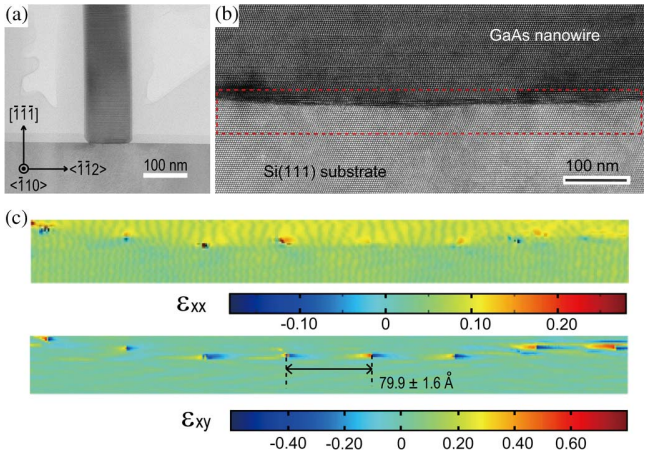

Fig. 12. (a) Low-magnified TEM image of GaAs NW on Si(1 1 1) substrate. The diameter of the interface is 103 nm. Incident direction of EB is in $\langle -1\,1\,0\rangle$ direction. (b) High-magnification image of (a). (c) ε_{xx} and $\varepsilon_{\mathrm{xy}}$ strain maps estimated from red-dashed square in (b).

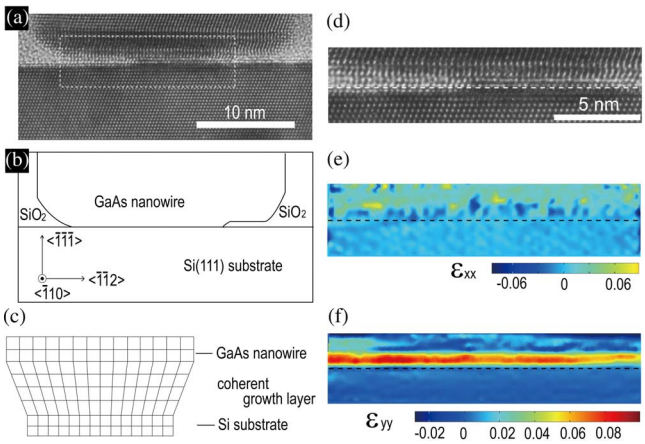

Fig. 13. (a) Cross-sectional TEM image of GaAs NW grown on Si(1 1 1). The NW diameter is 27 nm. Dashed rectangle shows region of heterojunction of GaAs and Si(1 1 1), which was 19 nm in diameter. (b) Illustration of TEM image of (a). (c) Description of coherent epitaxial growth. (d) Magnified image of dashed rectangle in (a). (e) ε_{xx} strain mapping calculated from image (d). Standard value for calculation is lattice constants of Si in the $\langle -1{-}12\rangle$ direction, i.e., $a_{\mathrm{Si}(x)} = 3.328$ Å. (f) ε_{yy} strain mapping estimated from image (d). Standard value for calculation is lattice constants of Si in vertical $\langle 1\,1\,1\rangle$ direction, i.e., $a_{\mathrm{Si}(y)} = 3.136$ Å. Adopted from [43] (Institute of Physics, copyright 2008).

shown in Fig. 12(c) is caused from the misfit dislocations. Note that any dislocation, such as threading dislocation, antiphase domains were not observed at the heterointerface. Therefore, such local strains accommodated the lattice mismatch in the GaAs/Si system as similar to the case of InAs NW on Si.

For the thin GaAs NWs, whose diameters were below 20 nm, periodic local strains were not observed. Fig. 13(a) shows TEM image of the heterointerface of the sample. SiO_2 was observed at the edge of the heterointerface of GaAs and Si, as illustrated in Fig. 13(b). This originated from the tapered sidewalls of the SiO_2 masks, which are formed due to the isotropic nature of etching with HF solutions. Thus, the actual opening diameter of the heterointerface is 19 nm [dashed rectangle in Fig. 13(a)]. The magnified image of the heterointerface shown in Fig. 13(d) reveals that the GaAs are epitaxially grown on the Si(1 1 1) surface. By using FFT and inverse FFT techniques (details written in Section II), the number of (1 1 1)A planes of the GaAs NW was estimated to 54 planes inside the opening, which was corresponds to that of the Si substrate. This means that coherent growth occurs without any misfit dislocations, as schematically shown in Fig. 13(c).

The GaAs NW was mapped with a strain of $+4.1\%$ in definition. The error in the strain calculation is approximately $\pm$ 0.5% strains ε_{xx}, in Fig. 13(e), were obtained very small in the first four MLs of a GaAs NW from the heterojunction and close to the value calculated for the Si substrate. This indicates that the lattice constant of GaAs in the $\langle 2\,{-}1\,{-}1\rangle$ direction in the four ML region is consistent with that of Si and the region has compressive strain. The ε_{yy} strain mapping of GaAs NW, on the other hand, shows lamellar tensile strain in the four ML region, and the amount is far larger than 4.1% The misfit strain ε_{yy} estimated from the lattice mismatch and elastic stiffness is $+3.7\%$ when ε_{xx} has compressive strain with -4.1% The estimated ε_{yy} becomes approximately $+7.9\%$ because the calculation of mapping is based on $a_{\mathrm{Si}(y)}$. This estimate is almost consistent with the value for lamellar tensile strain in Fig. 13(f). This means that the lattice constant of GaAs NW in the $\langle 1\,1\,1\rangle$ direction is increased at the heterointerface. Thus, the layer with compressive strain in the in-plane direction and tensile strain in the vertical direction compensates for the lattice mismatch. This concludes why GaAs NW grow coherently on the Si(1 1 1) substrate, as shown in Fig. 13(c), regardless of lattice mismatches.

In contrast to the case of the InAs NWs, periodical strains due to misfit dislocations were not observed in Fig. 13(e) and (f). This is because that the lattice mismatch in the GaAs/Si system is smaller than that in the InAs/Si system, and that opening diameter d_0 is sufficiently small for coherent NW growth. According to the calculations by Ertekin *et al.* [60] and Glas [61], the critical diameter for coherent NW growth is around 40 nm in case of GaAs/Si system (lattice mismatch is about 4.1%). Experimental results shown in Fig. 13 are within the theoretical coherent growth region. It should be noted that GaAs NWs with a larger diameter ($d > 40$ nm) are also formed that are extremely uniform, as shown in Fig. 9(b) and the results of Raman scattering in Fig. 9(c) indicated the absence of strains. It is still not clear whether these NWs contain misfit dislocations at the interface. Clarification of the boundary between coherent and incoherent growth as a function of d_0 is under investigation.

V. Integration of InAs NW-Based Vertical Surrounding-Gate Transistors on Si

In this section, integration of vertical III–V NW-based devices with Si substrate will be demonstrated. For InAs NWs on Si, we will focus on the fabrication of surrounding-gate transistors. Many groups have reported on lateral NW FET using scattered NWs as a channel [74]–[79], and some of them remark on the superior properties of these FETs to conventional FETs. However, there are few reports on NW FETs with vertical architecture because of the complicated 3-D device processing [80]–[83]. The epitaxially grown vertical NWs are geometrically suitable for high-density integration and for making a vertical

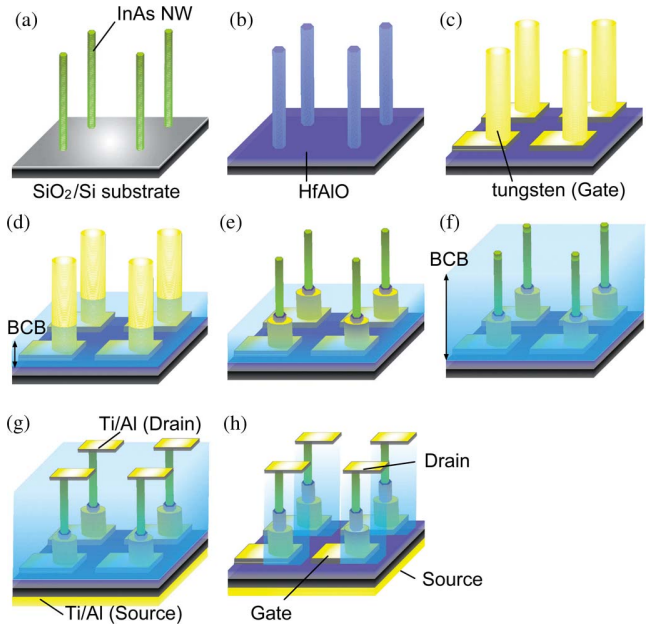

Fig. 14. Device fabrication processes. (a) SA-MOVPE growth of NWs. (b) ALD. (c) Surrounding-gate metal sputtering. (d) Etching stopper layer formation. (e) Selective etching of metal and high-k. (f) Electrical separation layer formation. (g) Drain and source metal evaporation. (h) Gate contacting-pads exposure. Adopted from [54] (Japan Society of Applied Physics, copyright 2010).

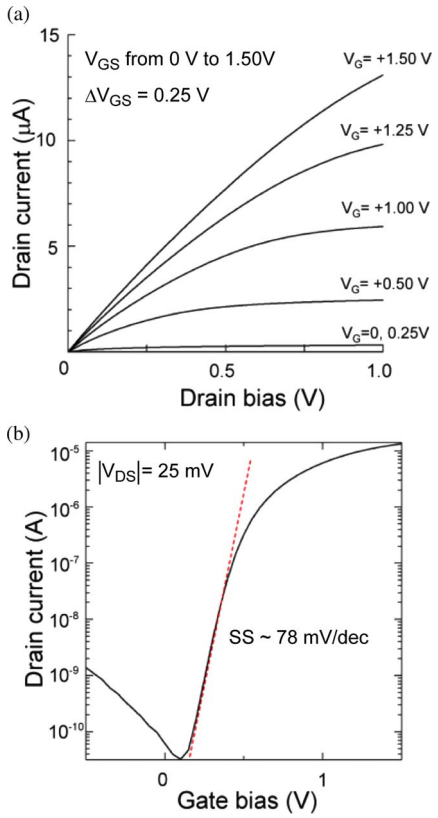

Fig. 15. DC characteristics of InAs NW-VSGT. (a) Output characteristics. (b) Transfer characteristics. Black lines are measured characteristics (at $V_{DS} = 1$ V).

surrounding-gate structure that suppresses short-channel effects effectively through excellent gate controllability, and InAs NWs are especially promising for use in electrical devices because small effective electron mass in InAs leads to high-electron mobility and because a Fermi level within the conduction band easily forms ohmic contact with various kinds of metals. InAs NW vertical surrounding-gate transistors (NW-VSGTs) thus have the potential to surpass conventional CMOS devices. Moreover, integration of the InAs NW-VSGTs on Si is promising for use of fast channels on Si-LSIs with nm-scaled occupied areas. Here, the fabrication and characterization of NW-VSGTs using InAs NWs grown on Si substrates will be demonstrated.

A. *Device Processes for InAs NW-VSGTs*

The VSGTs using single InAs NW grown on Si substrates have been made using high-k/metal surrounding gates. The device processes, shown in Fig. 14, were the same as previously reported in [54]. First, after the vertical NW growth [see Fig. 14(a)], the whole surface of NWs were covered with a 20-nm-thick layer of the high-k dielectric $Hf_{0.8}Al_{0.2}O_x$ formed by atomic-layer deposition (ALD) [see Fig. 14(b)]. Next, tungsten gate metal and its contacting pads were formed by RF sputtering and photolithography [see Fig. 14(c)]. It should be noted that the tungsten was deposited on both top surface and sidewalls of NW. Then, low-k benzocyclobutene (BCB) resin (Dow Chemical CYCLOTENE) was spin-coated once and etched back to the desired thickness (approximately 300 nm in this case) by RIE [see Fig. 14(d)], followed by dry and wet etching of the metal and high-k dielectric remaining on the top portions of the NWs. At this step, the BCB layer worked as a protection layer for etching, whose thickness defined the gate length L_G [see Fig. 14(e)]. After this, the devices were spin-coated again with BCB to electrically isolate the gate from the top drain electrode, and then, etched back by RIE to expose only top part of the NW [see Fig. 14(f)]. This process was for obtaining drain contact. Subsequently, the drain metal (Ti/Al/Ti/Au) and source metals (Ti/Al) were deposited on the top of NWs and bottom side of the substrate, respectively, [see Fig. 14(g)]. Finally, the gate contacting pads were exposed by RIE [see Fig. 14(h)].

B. *Output of the InAs NW VSGTs on Si Substrate*

The output and transfer characteristics of the device showing the best performances at RT are shown in Fig. 15(a) and (b), respectively. In this device, Si substrate is grounded and used as a common source. The measured FET properties were as follows: maximum drain current $I_{ds,\max} = 13.5\ \mu$A (at $V_{DS} = 1$ V), the peak transconductance $g_{m,\max}$ was 16 μS (at $V_{DS} = 1$ V), the subthreshold slope (SS) was 78 mV/decade (at $V_{DS} = 1$ V), the ON–OFF ratio $I_{\rm ON}/I_{\rm OFF}$ was 10^6 (with V_G window of 2 V), and threshold voltage $V_{\rm TH}$ was 0.2 V. $I_{ds,\max}$ and $g_{m,\max}$ were normalized with the gate circumference $w_g = 210$ nm (the NW diameter was about 70 nm), and given to be 64 μA/μm and 76 μS/μm, respectively. From the measured transconductance g_m, we calculated the field-effect mobility $\mu_{\rm FE}$ by using the formula $\mu_{\rm FE} = g_m L_G / C_{\rm OX} w_g (V_G - V_{\rm TH})$, where $C_{\rm OX}$ is the gate oxide capacitance of a cylindrical shape

was given by $C_{\mathrm{OX}} = 2\varepsilon_0\varepsilon_{\text{high-}k}/d_{\mathrm{NW}}\ \ln(1 + 2t_{\mathrm{ox}}/d_{\mathrm{NW}}) = 1.17 \times 10^{-2}\ \mathrm{F/m^2}$. $\varepsilon_{\text{high-}k}$ is relative permittivity (the value was calculated to 20.4 for $Hf_{0.8}Al_{0.2}O_2$ films by Maxwell–Garnett approximation), and t_{ox} is the thickness of the high-k dielectric ($t_{\mathrm{ox}} = 20$ nm) and we obtained a $\mu_{\mathrm{FE}} = 50\ \mathrm{cm^2/V \cdot s}$. This value is much less than the electron mobility of bulk InAs electron mobility, which is $33\,000\ \mathrm{cm^2/V \cdot s}$ at RT.

We think there are two main reasons for low μ_{FE}. One is interface states at InAs/HfAlO and the other is in a high-source resistance due to band offset at the interface between InAs NW and Si. With regard to the latter, we noticed that the current–voltage (I–V) characteristics between the source and drain were asymmetric with respect to $V_{DS} = 0$ V, particularly for large V_G, where the channel resistance is smaller. To minimize the effect of the high-source resistance, it is necessary to optimize the doping density of the Si substrate and InAs NW by band engineering, or to form a source electrode directly on the bottom of the NWs. The simulation value for drain current and transconductance were much larger than the experimental ones [54]. This is due to the too large mobility used in the simulation, but it is noted that the current does not scale with the value of mobility in the simulation. This suggests that the importance of velocity saturation in short-channel device. This makes the estimation of actual value of mobility difficult. In addition, the field-effect mobility was deduced neglecting the series resistance including access resistance by heteropotential barrier at Si/InAs interface. Interface states further reduce the transconductance and lower the estimated value of field-effect mobility. Therefore, we think obtained value of μ_{FE} is the lower bound of the mobility in our structure. For the core–shell NW approach, using an n-doped wider gap material as a shell structure also functions as an electron-supplying layer, therefore, we can achieve a modulation-doped InAs core channel, resulting in a HEMT. The devices were n-type single NW channel FETs having nonlinear characteristics due to the Si/InAs NW heteroband offset. The FET properties were comparable to those of other reported InAs NW-FETs, but there is still much scope for improvement.

VI. Monolithic Integration of Core–Multishell-NWs-Based LED on Si

One application of the III–V NWs on Si is in nanoscale light sources and detectors for on-chip integration, replacing Cu-based intrachip connections with high-performance optical interconnections in a small area. The large surface-to-volume ratio of the radial p-n junctions in core–multishell (CMS) NWs can make the junction area larger than that of planar substrate with the same surface area [84], [85]. The vertical CMS NWs with radial p-n junctions are therefore desirable because of their area effectiveness and they can improve the performance of LEDs, photodetectors, and solar cells. These CMS structures with radial p-n junction also have potential for avalanche breakdown with low-negative bias. The geometry of CMS NWs also makes them useful in free-standing NW-based APDs.

LEDs based on CMS NWs have been fabricated in wide bandgap semiconductors [85]–[88]. The NW-based light sources, which operated at wavelength from 800 to 900 nm, are suitable for on-chip integrations with Si-PDs and APDs system. However, there have been few investigations of III–V NWs-based LEDs on Si for the near-infrared region [39], [58]. In this section, we describe the integration of GaAs/AlGaAs CMS-NWs-based LEDs on Si substrate. The goal of fabricating CMS NWs is to make NW-based laser with current injections and free-standing NW APDs on Si platforms. This demonstration is a first step of our goals.

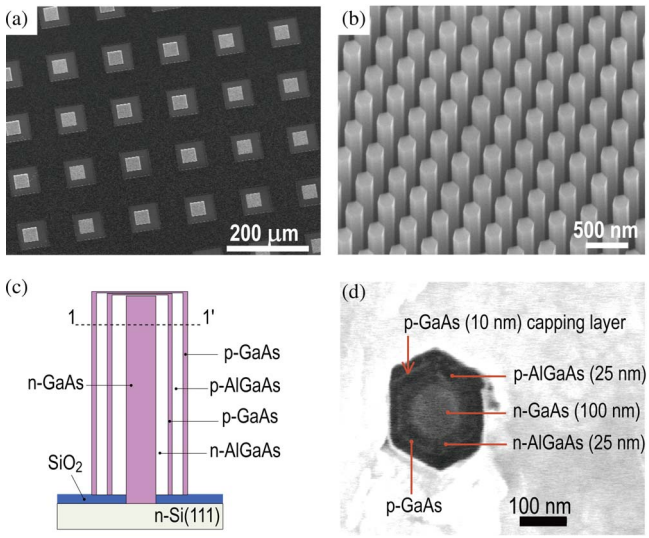

Fig. 16. (a) Overview of CMS-NW arrays on patterned substrate, (b) 30°-tilted view of SEM showing CMS NWs, and (c) illustration of CMS NWs (d) SEM image of a CMS NW cross-section cut following dashed line (1–1') in (c). Adopted from [58] (American Chemical Society, copyright 2010).

A. Growth of AlGaAs/GaAs Double Heterostructueres in CMS NWs on Si

We have designed and grown double-heterostructure (DH) CMS NWs on Si, as shown in Fig. 16(b). This is to enhance efficiencies in the NW-based LED. The structure consists of an n-type GaAs NW as a core and n-AlGaAs, p-GaAs, p-AlGaAs, and p-GaAs shells for the innermost to outermost shells, which are sequentially grown on the sidewall of the GaAs core NW. The n-type and p-type AlGaAs layers are cladding layers for confinements of electrons and holes in the inner p-GaAs layer and also for photons generated in the p-GaAs layers. The p-GaAs wedged between the n- and p-AlGaAs layers is quantum well (QW) tube, while the outer p-GaAs is a capping layer for ohmic contacts.

After the growth of the GaAs NWs, the n- and p-AlGaAs shell layers were formed at 700 °C for 5 min. The partial pressures of TMAl, TMGa, and AsH_3 were 1.2×10^{-6}, 8.2×10^{-7}, and 1.3×10^{-4} atm. The partial pressures of SiH_4 and DEZn were 2.5×10^{-8} and 2.8×10^{-6} atm for the n- and p-type layers, respectively. Also, the growths of the p-GaAs well layer and capping layer were performed at 700 °C for 3 min. Nominal carrier concentrations of planar GaAs and the p-GaAs were $3.5 \times 10^{17}\ \mathrm{cm^{-3}}$ and $4.0 \times 10^{18}\ \mathrm{cm^{-3}}$. The donor and acceptor concentrations N_D and N_A of planar n-AlGaAs and p-AlGaAs

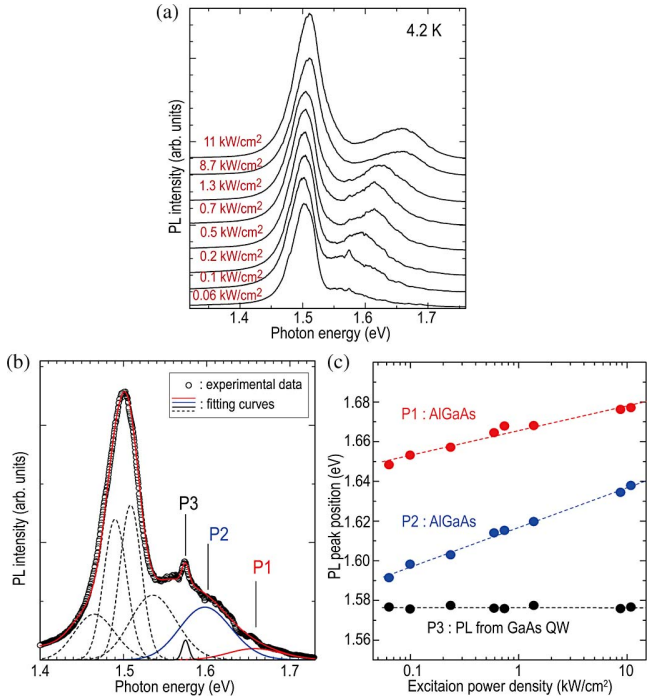

Fig. 17. (a) Curve fitting of typical PL spectrum. The excitation power density was 11 $\mathrm{kW/cm^2}$. Opened white circles show experimental data, dashed lines are fitted curves for GaAs NW. Red (P1), blue (P2), and black (P3) solid lines are for shell layers. Inset depicts typical PL spectrum under weak excitation ($0.1\ \mathrm{kW/cm^2}$). (b) PL spectra for the CMS NWs with variation of excitation power density. (c) Excitation power dependence of PL peak positions for P1 (closed red circles), P2 (closed blue circles), and P3 (closed black circles). Adopted from [58] (American Chemical Society, copyright 2010).

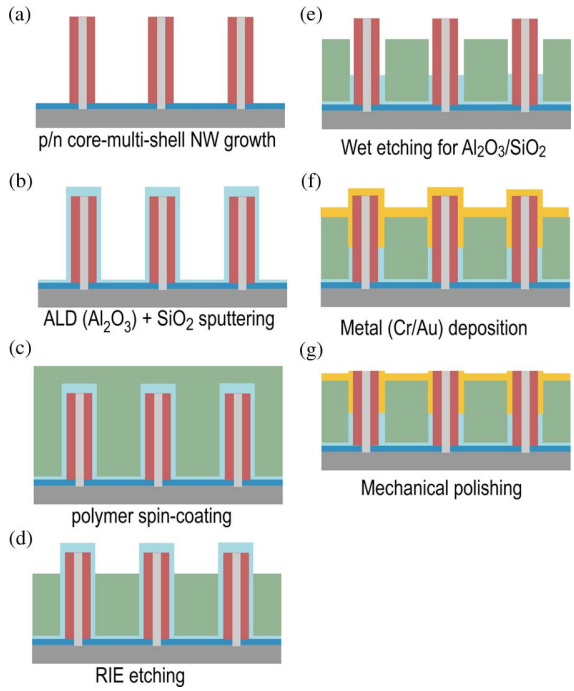

Fig. 18. Schematic illustrations for fabrication process of vertical NW-based LEDs. (a) SAG of CMS NWs with p-n junction on Si. (b) Deposition of Al_2O_3 (20 nm) by ALD, and SiO_2 (50 nm) by RF sputtering. (c) Spin-coating of polymer. (d) RIE etching for top parts of the NWs. (e) Wet etching for Al_2O_3/SiO_2 by BHF solution. (f) Metal (Cr/Au) deposition. (g) Mechanical polishing for top parts of the metal-coated NWs.

were 9.0×10^{17} and 1.0×10^{18} $\mathrm{cm^{-3}}$. The actual doping level in each layer of the CMS NWs is unclear because of the difficulty in characterizing such thin layers. As mentioned in previous report regarding core–shell InP NW solar cell [90], there is a possibility that these carrier concentrations for the CMS NWs were lower than those for the planar epitaxial layers.

Fig. 16(a) and (b) shows the growth results of the DH structure CMS-NW array on Si. Vertically aligned regular hexagonal NWs with diameter d of 250 nm were fabricated on Si substrate. Formation of kink and taper on the NW sidewalls resulted from high doping were not observed in these images. Thus, each NW had uniform shell layer thickness. The average heights were 3 μm. Fig. 16(c) is an illustration of the CMS-NW structure and Fig. 16(d) shows an SEM image taken from a cleaved and selectively etched CMS NW. In this image, the lateral thicknesses of both n- and p-AlGaAs layers are 25 nm, and the lateral growth rate was estimated to be 2.5 nm/min.

B. Optical Properties in DH CMS NWs With Radial p-n Junctions

Fig. 17(a) shows the PL spectra of the CMS NWs at 4.2 K under various excitation power densities. First, curve fitting with the Gaussian functions for Fig. 17(b) shows two main peaks at 1.654 eV (P1) with a full width at half maximum (FWHM) of 74 meV and 1.598 eV (P2) with FWHM of 72 meV. Also, additional sharp PL peak resulting from GaAs QW layer is observed at 1.574 eV (P3) with FWHM of 8 meV. The value of the energy shift for P1 corresponds to that of a Zn-related donor–acceptor pair (DAP) transition [91] and P2 is thought to be the Si–C related DAP transition in the AlGaAs cladding layer [92]. Fig. 17(c) indicates that the peaks P1 and P2 were blue-shifted with increased excitation power density, and P3 was still constant with increment of the excitation powers. The P1 and P2 are thought to be DAP luminescence. The Al composition in the AlGaAs shell is estimated at 12%, taking into account the donor and acceptor levels. The PL from the GaAs QW is clearly observed at 1.574 eV for weak excitation, as shown in Fig. 17(b). The FWHM from the peak deconvolution for the PL is 8 meV. This narrow linewidth reflects exciton emission from the GaAs QW. From the PL peak energy, thickness of the GaAs QW is estimated to be 7 nm by using Schrödinger's equation with simple rectangular-shaped well.

C. Device Processes for Vertical NW-Based LEDs

The NW-based LEDs were fabricated using the DH CMS NWs on Si. Detailed processes are illustrated in Fig. 18. First, $SiO_2\,(50\ \mathrm{nm})/Al_2O_3\,(20\ \mathrm{nm})$ were deposited on the NW surface to avoid RIE-induced damage as well as to make a slit around the NW sidewalls. The SiO_2 was deposited by RF sputtering and the Al_2O_3 was formed using ALD. Next, the sample was buried with polyresin, and etched with RIE to expose the top parts of the NWs for metal contacts. After the RIE, SiO_2/Al_2O_3 was removed by BHF solution and 70-nm-wide slit was formed around the CMS NWs. The depth of the slit was 1.5 μm. Then,

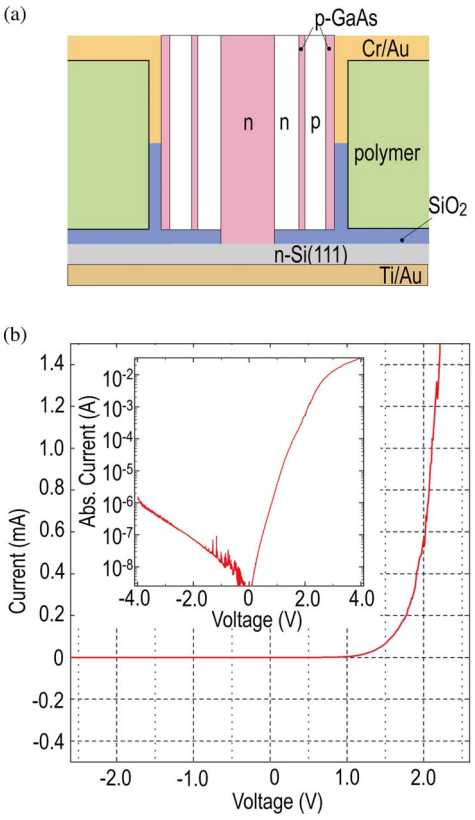

Fig. 19. (a) Illustration of CMS–NW-based LED structure. (b) *I–V* curves. Inset shows the semilogarithmic plots for the *I–V* curves. Adopted from [58] (American Chemical Society, copyright 2010).

Cr/Au metal was deposited onto the top parts of the RIE-etched NWs. In the metal deposition, we used the rotating sample holder to effectively coat the metals on the sidewalls of the CMS NWs. The rotation per minute was 50. Also, the wafer was tilted to about 5°. This is for depositing the metal into the deep slit around the NW sidewalls as much as possible. It should be noted that space of a slit was not completely buried by Cr/Au metals. After deposition of the Cr/Au metal, the top parts of the NWs were mechanically ground to make wrapped metal contacts on NW sidewalls only. We used Ti(20 nm)/Au(100 nm) metal and silver for backside electrode.

D. Performance of CMS-NW-Based LEDs on Si

Fig. 19(a) illustrates the NW-based LED structure. The Cr/Au thicknesses was Cr(10 nm)/Au(130 nm) metal with 25-nm-thick n- and p-AlGaAs shell layer. In this LED structures, about 2×10^5 NWs are connected in parallel. The total junction area is estimated to be 1.3×10^{-3} cm^2. To determine the recombination mechanism in the CMS-NW-based LED on Si, we measured the current of the CMS-NW devices at voltages from -4 to 4 V using an HP 4156B parameter analyzer. In these measurements, the Cr/Au metal was positively biased, and the Ti/Au backside electrode was grounded. Fig. 19(b) shows the *I–V* curves for these structures. The curves for all devices show moderate rectifying properties. The inset of the Fig. 19(b) shows a semilogarithm plot of the *I–V* properties. In this structure, the depletion width is estimated to be 23 nm and the total thickness of this CMS layer was thicker than the depletion width.

The rectifying curves for the CMS-NW-based LED array with thick AlGaAs layers indicate gradual linear curves resulting from unexpected resistance. The resistances originated from series and shunt resistance across the NWs and Si substrate. Also, premature turn-ON behavior originating from surface states occurred. Considering these resistance (R_S) with the CMS-NW-based LED and shunt resistance to be infinity, the current equation is expressed as $J(n) = J_0 \exp[(V - R_S I)/nkT]$, where n is the ideality factor of the p-n junction. From this equation, the n is estimated to be 3.8 for the device, and the R_S is calculated to be 45.3 Ω. The ideality factors for the device is higher than conventional GaAs-based diode ($n = 1.1$–1.5), and also higher than the thermal diffusion or recombination expected from the Sah–Noyce Schottky mode [93]. Such high-ideality factors are usually observed for AlGaN-based diodes [94], [95]. The reason for such high value of the ideality factor is thought to be the carrier tunneling across the junction.

The *I–V* curve indicates leakage current in the negative-bias region. It should be noted that this behavior was not observed for CMS NWs on GaAs(1 1 1)B substrate (not shown here). This is because of the band discontinuity across the GaAs/Si junction. Heterojunction between III–V NW and Si forms band discontinuity. Several reports have investigated the valence and conduction band offset with photoemission spectroscopy [96], [97]. Potential barrier of the band offset leads to Schottky properties. The Schottky properties of III–V NW on Si have been reported. The discontinuity across the GaAs/Si junction would be affected by several factors, such as misfit dislocations, interface states, and the conductance of Si and III–V NWs. Further investigations are required to clarify this discontinuity across the III–V NWs/Si junctions and to further improve the performance of III–V NWs-based devices on Si.

Fig. 20(a) shows the typical electroluminescence (EL) spectra obtained under several current conditions. The threshold current for EL is 0.5 mA (current density is 0.3 A/cm^2) at 1.9 V. The EL peak position is around 1.48 eV. The EL peak position is shifted to 60 meV from that of the GaAs bandgap at RT ($E_g = 1.42$ eV). This EL came from the DH structures, because the estimated width of the GaAs QW tube is 7 nm, which is consistent with the value estimated from the LT PL spectra shown in Fig. 17(b). The FWHM of the EL is 130 meV, which is larger than the theoretical linewidth (1.8 *kT*) in LED spectra and PL spectra at RT also showed large FWHM. This is therefore because the EL spectra in Fig. 20(a) contain several luminescence centers resulting from DAP transitions from Si, C, and Zn impurities in the AlGaAs layers.

The EL intensity increased superlinearly with the current injection, and it was saturated from $I = 1.5$ mA (1.2 A/cm^2), as shown in Fig. 20. The superlinear characteristic in the EL intensity at low-current injection indicates the CMS-NW-based LED is similar to that of superluminescence LED [98]. This is thought to be because the AlGaAs shell layer surrounded by Cr/Au metal and oxides acts as a kind of waveguide because the reflectivity of the metal is above 95%. The origin of the saturation was the carrier overflow as observed in surface-emitting

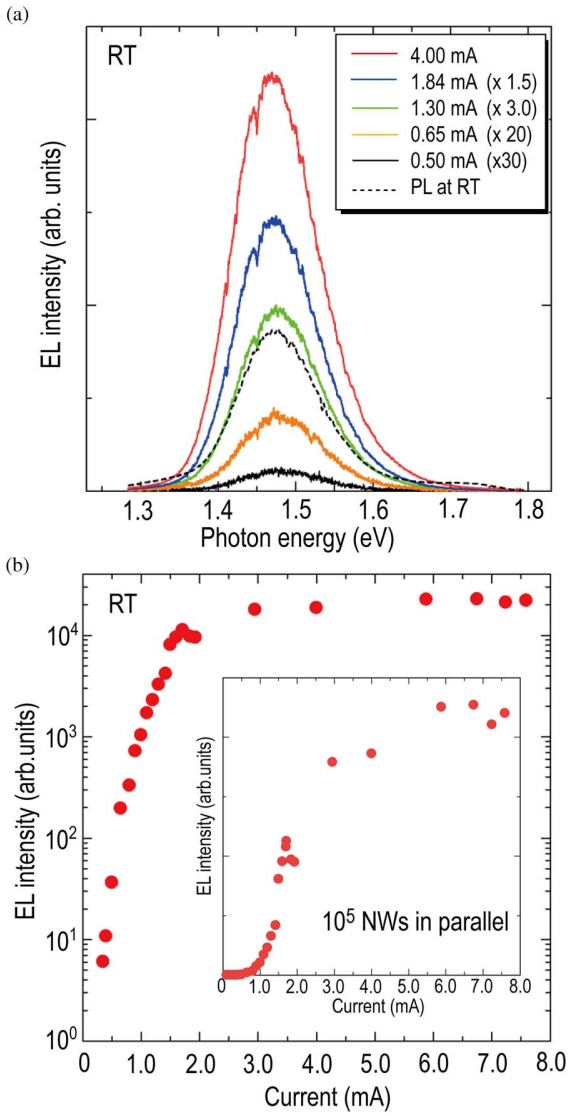

Fig. 20. (a) EL spectra under several current injections at RT. Solid lines indicate the EL, and the dashed line spectrum depicts the PL at RT. (b) Semilogarithm plot of EL intensity as a function of injected current. Inset depicts linear plot of the EL intensity. Adopted from [58] (American Chemical Society, copyright 2010).

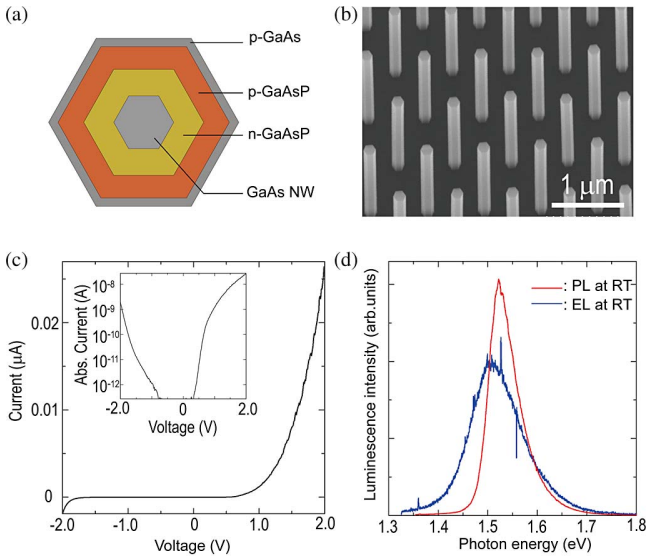

Fig. 21. (a) Illustration of cross section for GaAsP/GaAs CMS NW. (b) Growth results of the GaAsP/GaAs CMS NWs. (c) *I–V* property for the CMS NWs. Inset shows the semilogarithmic plots for the *I–V* curves. (d) EL (blue-colored line) and PL (red-colored line) spectra of the CMS NWs.

LEDs. This is because the volume of the active region in the CMS NWs is very thin and parasitic resistance (contact resistance, series resistance, etc.) is high. Moreover, no shift of the EL peak position resulting from Joule heating on the junction temperature was observed when further increasing the current injections. This is because the Si substrate acts as a heat sink due to its good thermal conductivity as compared to III–V compound semiconductors. This heterogeneous integration can, therefore, lead to thermally stable driving. However, the thermal conductivity for the BCB resin is still low. Generally, GaAs-based LEDs fabricated on Si, without buffering do not achieve such bright EL because of threading dislocations resulting from the thermal coefficient difference. Reduction of threading dislocations using SAG [9] has been reported, and we also found that InAs and GaAs NWs grown on Si contained no threading dislocations [30], [43]. The nm-scaled selective-area technique, therefore, could control the generation of threading dislocations and produce better performing CMS-NW-based LEDs directly grown on Si surfaces without buffering techniques.

E. Fabrication of GaAsP/GaAs CMS Structures and Multi-QW Layers Inside the CMS NWs

One reason for using CMS NWs for optical devices is to make LDs and APDs using NWs. As mentioned earlier, a free-standing CMS NW has geometrical advantages with regard to junction area and self-cavity effects. The AlGaAs/GaAs systems are not good materials for light-emitting devices because of the rapid degradation resulting from generation of defects, such as dark-line dislocations and dark-spot defects [99]–[102]. There are several approaches to make light-emitting devices without such dislocations and defects. One is to use other material systems, and the other is to use multi-QWs structures to enhance the optical gain [103]. Here, we demonstrate on the fabrication of GaAsP/GaAs CMS-NW-based LEDs on Si and AlGaAs/20QWs/AlGaAs CMS-NW-based LED array on Si as a first step for achievement of NW-based LDs. The P-related III–V semiconductors are thermally stable against Joule heating with high-current injections that leads to suppress formation of dark-line dislocations. The multi-QWs are effective to enhance the optical gain.

As shown in Fig. 21(a), we have designed and grown simple GaAsP/GaAs CMS-NW-based LEDs on Si. Their structure consists of an n-type GaAs NW as a core and n-GaAsP, p-GaAsP, and p-GaAs shells. Tertiarybutyl-phosphine (TBP) was used for the P-source material. The n-GaAsP and p-GaAsP were grown at 650 °C. p-GaAs cap layer was grown at 700 °C. The partial pressures of SiH_4 and DEZn were 2.5×10^{-8} and 2.8×10^{-6} atm for the n- and p-type layers, respectively. The growth

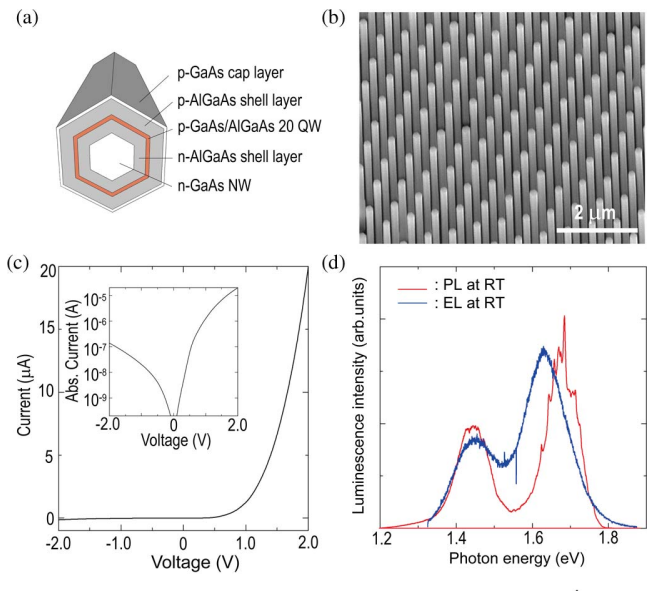

Fig. 22. (a) Illustration of cross section for AlGaAs/20QWs/AlGaAs CMS NW. (b) Growth results of the CMS NWs. (c) *I–V* property for the CMS NWs. Inset shows the semilogarithmic plots for the *I–V* curves. (d) EL (blue-colored line) and PL (red-colored line) spectra of the CMS NWs.

conditions for the AlGaAs/QWs/AlGaAs CMS-NW-based LED array on Si were same as those for the GaAs/AlGaAs CMS-NW-based LED. As for the QWs, we have designed the 20-layers AlGaAs/GaAs multiple QW (20-QWs) with the separation of 10-nm-thick $Al_{0.12}Ga_{0.88}As$ layers. The thickness of the GaAs well layers was constant for approximately 7 nm. The device processes were same as those of GaAs/AlGaAs CMS-NW-based LED arrays on Si.

The electrical properties and EL spectra of GaAsP/GaAs CMS-NW-based LED on Si are shown in Fig. 21(c) and (d). The *I–V* curve showed Shottky-like behavior resulting from the insufficient doping for GaAsP layers and some leakages. The LED based on GaAsP/GaAs CMS NWs showed rectifying properties with the ideality factor of 1.59. The R_s was 14.6 MΩ. Although, the devices showed high R_s, the ideality factor was close to that of commercially available GaAs LED. The transport property in this device thought to be based on diffusion current process. EL was observed at around 1.51 eV at RT. The red-colored solid line in Fig. 21(d) shows the PL spectrum from same sample at RT. The luminescent peaks were the same as that of the EL peak, which means the current injection occurred across the p-n junction in the GaAsP regions. The threshold current for the EL was 0.08 μA, but the bias voltage was 2.5 V. This is because of high-contact resistance through Shottky contacts. The moderate rectifying properties of AlGaAs/20-QWs/AlGaAs CMS-NW-based LED array on Si are evident in Fig. 22(c). The ideality factor for the device was 1.93 and R_s was 50 kΩ. Such high resistance was thought to be from band offsets in the GaAs/AlGaAs multi-QW layers. The transport property in this device was recombination current process. The EL peaks were observed at 1.45 and 1.65 eV. The former was due to the GaAs QW layers and latter due to the AlGaAs barriers inside the multi-QWs. The threshold current was 20 μA at 2.0 V. Red-colored solid line in Fig. 22(d) show the PL spectra at RT. The PL spectra showed small oscillation due to cavity effect in multi-QW layers like a Bragg reflectors at around 1.65 eV, which means these structures have potential for the confinement of photons inside the NW. Further improvements in heat management, refractive index, and contact resistance are required for LD applications.

VII. Conclusion

We have reviewed and reported on recent progresses in the growth of III–V NWs on Si by SA-MOVPE and on device applications. We have focused on the As-related III–V NWs on Si substrate because these materials are expected to be used in high-performance NW-based electronic and optical devices.

The key techniques for controlling growth direction for III–V NWs on Si substrate have been found to form an (1 1 1)B surface on the nonpolar Si surface and to suppress the thermal desorption of group-III atoms. These approaches were effective for the SAG. The techniques used align vertical III–V NWs on Si should, therefore, help to open new fields of III–V/Si integration.

We have also described the fabrication of VSGTs and vertical CMS-NW LEDs on Si substrates. These devices could be well suited to a trend of next-generation electronics and photonics on Si platforms, but many problems, such as band discontinuity across the III–V NW and Si heterojunctions, unexpected doping from Si substrate, misfit dislocations across the junction, and in coherent growth must be solved. We, therefore, have to investigate such unclear issues further and improve the device structures. Recently, unique photovoltaic device using band discontinuities in III–V/Si heterojunctions have been reported. Next generation of III–V NW/Si integration is required for such new concepts.

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