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# Improved Allegro to Pro/E Bidirectional Data Exchange

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Introduction

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## **IDF** (Intermediate Data Format)

## IDF 2.0, 1993

Specification consists of two files. A board outline file and a component placement file. Files contained basic information about the shape of the board, the position and size of plated and non-plated circular holes on the board, and the position and basic shape of the components on the board.

## IDF 3.0, 1996

Added support for manufacturing panels with the same features as the board specification. Also added support for more keep-out and outline types, placement areas, and owner properties. The two formats are very similar in structure and content. This is the current specification that is used as a data exchange basis by Cadence and PTC, Pro/Engineer.

## IDF 4.0, 1998 (Never adopted)

File format brought the ability to interchange much more detailed information. IDF 4.0 files contain information about board features such as land patterns, pads, vias and copper filled areas which aren't supported by IDF 2.0 and 3.0. The IDF 4.0 format also allows entities to be defined in much more detail than the previous versions of the specification.



## **Data Representation**

## IDF 3.0 Exchange Format

Board Outline - Including Cutouts

Holes

Keepout Areas

Keepin Areas

**Component Placement** 



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uf88	37a00.brd	THOU						
. ENI	_HEADER							
. BO	ARD_OUTLINE	ECAD						
	62.00							
0	4820.00	-130.0	0.0	000				
0	4820.00	1533.0	0.0	000				
0	-130.00	1533.0	0.0	000				
0	-130.00	-130.0	0.0	000				
0	4820.00	-130.0	0.0	000				
1	1876.00	835.0	0.0	000				
1	1876.00	715.0	00 180.0	000				
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1	1976.00	835.0	00 180.0	000				
1	1876.00	835.0	0.0	000				
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.PL	ACE_KEEPOUI	ECAD						
TOP	283.0	0						
0	3332.00	270.0	0.0	000				
0	3332.00	-130.0	0.0	000				
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	205.00	236.00	0.00		0.000	TOP	PLACE	D
CON	USB_4P_RTF	_SHLD_TH_S	SLT W6307	USB_FN	IT_A			
	791.00	236.00	0.00		0.000	TOP	PLACE	D
CON	HDR_2X20_S	HR_2MMK21	U6602 FN	r_pnl				
:	3500.00	1350.00	0.00	18	0.000	TOP	PLACE	D
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## **Translation Process**

The IDF data exchange process can originate in either Pro/Engineer or Allegro.





### **Best practice:**

MCAD creates Board Outline and data is imported into Allegro

ECAD places parts and exports data to MCAD.

#### **Problem:**

Keep-out areas associated with the Allegro symbols will be disassociated from the symbols during import in Pro/Engineer.



Coordinate systems are used to identify and to calculate location coordinates in the IDF file.

The coordinate system in Pro/Engineer for the board outline is defined by the ECAD\_DEFAULT coordinate system. The import process from Allegro to Pro/Engineer for the board outline is dependent on the 0,0 location in Allegro as a reference point to the ECAD\_DEFAULT coordinate system in Pro/Engineer.





## **Translation Process - Parts**



During the import into Pro/Engineer, placement coordinates for parts that are created in Pro/Engineer are calculated based on the ECAD\_DEFAULT coordinate system on the Pro/Engineer part referenced to the ECAD\_DEFAULT coordinate system on the PCB part. For extruded parts the symbol origin defined in Allegro is used as a reference to the ECAD\_DEFAULT coordinate system on the PCB part.

The coordinate systems for the components in each application must match in order for the import/export exchange to be accurate.



## **Translation Process - Holes**

Representation of holes in the IDF transfer can be confusing. Holes in Allegro are represented by symbols. In Pro/Engineer they are features or cuts in the PCB part. The best practice is to model holes in Allegro and use ECAD Parameters in Pro/Engineer to influence the definitions in the exported IDF file.





When exporting holes from Allegro PCB Editor, depending on the value of the IDF\_OWNER property, the export results will differ. The Allegro PCB Editor will export ECAD owned or UNOWNED holes as an entry in the .DRILLED\_HOLES section of the IDF file as well as an entry in the .PLACEMENT section.

If the IDF\_OWNER property on a hole symbol in Allegro is set to MCAD, the hole will only appear in the .DRILLED\_HOLE section of the IDF file exported from Allegro. The hole will be imported in Pro/Engineer as a 3D cut through the PCB.



## **Translation Process - Holes**

An IDF 3.0 drilled hole record contains the following fields:

| DIA |X | Y | PLATING | ASSOC | TYPE | OWNER |

DRILLED HOLES. 40.00000 2000.00000 2000.00000 NPTH BOARD PIN MCAD 40.00000 2165.00000 2000.00000 PTH BOARD VIA MCAD 40.00000 2165.00000 2330.00000 NPTH BOARD MTG MCAD 40.00000 2000.00000 2330.00000 PTH BOARD TOOL MCAD 125.00000 9750.00000 250.00000 NPTH BOARD 150C125 MCAD 60.00000 750.00000 250.00000 NPTH P1 OTHER MCAD 60.00000 850.00000 250.00000 NPTH P1 OTHER MCAD .END DRILLED HOLES

The following naming formula is used to create hole symbols in Allegro during the IDF import:

#### <(N)on-plated or (P)lated> + <TYPE> + <diameter in mil \* 10>

The example above will result in the following symbols and pad stacks in the Allegro PCB database as a result of the IDF import:

NPIN400, PVIA400, NMTG400, PTOOL400, 150C125

Allegro symbols will be placed for holes with reference designators.



# **Translation Process - Holes**

BOARD_01 (Active) - Pro/ENGINEER		
Eile Edit View Insert Analysis Info Applications Tools Window Help	-	
	×¥×	<b>N</b> ?
BOARD_CITPRT BOARD_CITPRT PROTUNESON id 33 CS0 CS1 T Hole 1 T Hole 2 T Hole 3 T Hole 3 T Hole 4 T ISERT Here BOARD_CITPRT CAD_PLATIN ECAD_HOLE PROTUNESON id 33 CS0 CS1 T Hole 1 T Hole 1 T Hole 3 T OLL PTH MCAD T Hole 3 T OLL PTH MCAD T Hole 3 T OLL PTH MCAD T Hole 4 T ISERT HERE CSC CSC CSC CSC CSC CSC CSC CS		
Datum points will not be displayed.		^
Coordinate Systems will not be displayed.     Axes will not be displayed.     Datum planes will not be displayed.     Smart	× 8	



Three solutions for hole definition:

- 1. Modify the value of the hole TYPE in Pro/Engineer to use an existing Allegro symbol name.
- 2. Build an Allegro library with full-featured padstacks using the naming convention of the IDF 3. 0 specification.
- 3. Manually replace all hole symbols with existing library symbols after importing the IDF file into Allegro.





The current IDF 3.0 based interface is not robust enough to translate Cadence Allegro® 2D data to Pro/Engineer® 3D data without extensive knowledge of the interface and outside configuration files.

Limitations in the specification and limitations of the IDF implementation in Allegro and Pro/Engineer make the current exchange of data difficult without extensive knowledge of the IDF 3.0 specification and the specific implementation of the specification in the tools.



Keep-out areas and PLACE\_BOUND\_TOP shapes can only be drawn as closed polygons.

Time consuming manual edits have to be made to create voids and cavities in keep-out areas.

This limitation is due to the fact that Allegro PCB Editor does not allow voids in keep-out areas.





Individual keep-out areas are required that represent different heights. The ability to use stacked keep-out areas or define different heights in keep-out areas is necessary in most designs.

The image below illustrates how the housing of a component defines different height restrictions. These areas have to be created as either overlapping or stacked placement keep-out areas in Allegro and/or Pro/Engineer.





BOARD1 (Active) - Pro/ENGINEER





- Currently only the PLACE BOUND TOP subclass can have a height that is • transferred to Pro/Engineer and extruded as a 3D solid due to IDF 3.0 limitations.
- If a PLACE BOUND BOTTOM shape is used, the PLACE BOUND TOP and PLACE\_BOUND\_BOTTOM shapes are merged into one shape in the Allegro IDF export file. The merged shape is used as the basis for the extruded component in Pro/Engineer.





- Use the PLACE\_BOUND\_TOP and PLACE\_BOUND\_BOTTOM subclasses to draw the boundaries as you normally would in Allegro.
- Allegro allows the user to specify which subclass to use for PLACE\_BOUND\_TOP and PLACE\_BOUND\_BOTTOM.
- Define a layer class for the top and bottom component boundaries. In this example we use:
- IDF\_PLCB\_BOTTOM and IDF\_PLCB\_TOP.
- Draw the top component boundaries on the user defined layer subclass, IDF\_PLCB\_TOP, for the top IDF output. *Do not use* the IDF\_PLCB\_BOTTOM subclass.





The subclass names for the IDF export can be set in the User Preferences in Allegro. The user defined bottom subclass IDF\_PLCB\_BOTTOM will have nothing on it. This will override anything that may be on the PLACE\_BOUND\_BOTTOM subclass.

📴 User Preferences Editor 📃 🗆 🔀							
Categories	Category: Idf						
Artwork	Preference	Value	Effective				
Autosave	idf_ignore_comp_height:		Command				
Browser	idf_ignore_part_number:		Command				
Control_panel	idf_nodelete:		Command				
Design_partitic	idf_place_bounds_bottom:	IDF_PLCB_BOTTOM	Command				
Dfa_drc	idf_place_bounds_top:	IDF_PLCB_TOP	Command				
Display							



The result in Pro/Engineer will be an extrusion represented by the combination of outline on the IDF\_PLCB\_TOP and the PACKAGE\_HEIGHT\_MAX assigned to the PLACE\_BOUND\_TOP area in Allegro.



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# **Current IDF 3.0 Limitations - Symbol and Part Modeling**

# Model every part in Pro/Engineer and Allegro

#### **Pros:**

A complete MCAD-ECAD library that ensures exact data exchange.

#### Cons:

The creation and maintenance of models is labor intensive and error prone.

Part representations must be synchronized either manually or buy using a revision control or PDM system.



# **Current IDF 3.0 Limitations - Symbol and Part Modeling**

## Don't model any parts. Use only the part extrusion.

#### **Pros:**

No library maintenance symbol cross reference necessary. All part extrusions come from PLACE\_BOUND\_TOP, COMPONENT\_HEIGHT\_MAX in Allegro footprints.

### Cons:

All part extrusions come from PLACE\_BOUND\_TOP, COMPONENT\_HEIGHT\_MAX in Allegro footprints. Model accuracy depends completely on the PLACE\_BOUND\_TOP definition.



## **Current IDF 3.0 Limitations - Symbol and Part Modeling**

## Model critical parts in Pro/Engineer. Non-critical parts extruded.

## **Pros:**

Only Critical parts are modeled in Pro/Engineer and Allegro for minimum overhead.

Non-critical part extrusions are defined from PLACE\_BOUND\_TOP subclass and the COMPONENT\_HEIGHT\_MAX attached to the PLACE\_BOUND\_TOP subclass.

## Cons:

# Extrusion height dependent on definitions from Allegro footprints or pre-defined height.

Non-critical part height extrusions come <u>only</u> from PLACE\_BOUND\_TOP subclass in Allegro footprints. Extrusions default to a defined setting when the data is created from Allegro if there is not a COMPONENT\_HEIGHT\_MAX defined in Allegro. Place boundaries in Allegro do not always represent the exact part outline.

# This method seems to be the best balance of part representation and maintenance.



Package keep-out areas assigned at the board level in Allegro can be used to represent bottom side height restricted areas.



The keep-out area in the above example represents the length of the bottom side pins of the connector plus some tolerance.

The problem with this method is the non-associability of PLACE KEEPOUT areas and the component they belong to.



This example shows how and inference analysis can reveal a board assembled too close to the housing of the product using a PACKAGE KEEPOUT area.





 In the example below the PLACE\_BOUND\_TOP area had to be created with a small void, the black line across the PLACE\_BOUND\_TOP outline, to allow the Package KEEPOUT area Max Height to be less than the PLACE\_BOUND\_TOP Max Height. A Min and Max height that describes the component areas more completely is needed.





- A method is needed to describe areas that may contain one part type or multiple part types in the PCB database.
- Assignment of rooms at the schematic level can be used to define parts that are allowed in the room.
- An easier approach would be to be able to assign the parts to a room in the PCB database. If the room definition could have a height attribute, there could be an interference check at the board level without having to assign a duplicate component keep-out area.
- Additionally there is a need to be able to constrain overlapping rooms or keep-out areas where the height and component type restrictions may apply.
- Primary area is .3 max height. An area in the middle is .1 max height. Symbols to be placed in the .1 area need to be limited by height and symbol type or reference designator.
- For example; only capacitors and resistors less than .1 can be placed inside the area.



# **Entity Representation**

• The current IDF 3.0 implementation in Allegro PCB Editor uses reference designators to associate parts between the PCB and the mechanical model.

# A better approach would be to represent each entity with an object reference assigned during the intermediate file creation.

- The IDF 4.0 data model is based on a hierarchy of assemblies, parts, and features. Assemblies are constructed from instances of parts and other assemblies. Parts are constructed from features.
- Features define the geometric shape and other physical characteristics of parts, and convey functional information as well. IDF 4.0 also provides figures, footprints, and sub-layouts to represent associations among instances and features that are useful to maintain during the design of the PCA.
- This example may not be the ultimate answer to the data model. It is used here as an example of an object oriented hierarchy that would work better than the current IDF 3.0 data model.



# So ... What Now?





## So... What Now?

### What do we need in an Electrical/Mechanical Interface?

#### Easy to use

- Match entities in both mechanical and electrical packages as closely as possible using extrusions.
- Simplify the association of part representations between systems.

#### **Better representation of entities**

- Entities not tied to Reference Designators. Use object references.
- XML or similar structure so that entity definition can be extendible.
- More extensive model attributes and properties exposed in Pro/Engineer.
- Ability to add multiple attributes to restricted areas for easier specification of areas.
- Min/Max Height of components from PCB database.

#### Ability to use the data in multiple disciplines

- Mechanical, Thermal, Electrical, Signal Integrity
- Based on what users need... Not a specification...



# **The Future**



## **Improved Electro-Mechanical Co-Design Process**

### **MCAD-ECAD** Collaboration



## How does it work?



#### Verify Changes

"What actually did change?"



# **Key Technologies**

#### **IDX File**

- XML structures based on the EDMD schema from ProSTEP (open industry standard)
- Incremental changes data only, no design meta data
- Can be used as an IDF replacement for initial board/component transfer from MCAD to ECAD
- Each change description contains:
  - A unique change ID
  - Reference to objects involved by unique IDs
  - All change data including ownership
  - Change status: proposed, accepted, rejected - with traceability (user, date, etc)
- Can be looked at as a tool-agnostic format for "intelligent" annotations/markups
- Will be understood by Windchill

#### ProductView Validate

- A normalized way to "see" a change without the context of design data
- Same look and feel for all tools
- Displays content of the IDX file in a tabular form
- Cross-Highlights changes to the authoring or visualization tools (sand-box)
- Allows to declare a new change status (propose > reject/accept)
- Will become part of Windchill

Replacing full design swaps with exchange of incremental changes



# **PV Validate – Managing Change**

Validation Manager 3.0									
<u>F</u> ile <u>E</u> dit <u>T</u> ools <u>H</u> elp									
Transactions	Selected Transactions (Filtered 6 of 9)					Transaction Details			
	Filter: Modified By	~	rplante	F	ind Clear	Attribut	te / Property 🛓	Current	Baseline
<ul> <li>All (15)</li> <li>Added (2)</li> <li>Component (1)</li> <li>Net (1)</li> <li>Removed (1)</li> <li>Variant (6)</li> <li>Component (6)</li> <li>Variant - Geometric (4)</li> <li>Top (6)</li> <li>Sublayer Name (4)</li> </ul>	<ul> <li>▼ Type</li> <li>✓ Variant Component</li> <li>✓ Variant Component</li> <li>Unique Component</li> <li>Added Component</li> <li>Added Net</li> <li>Removed Compnent</li> </ul>	Object U100 C25 A12 C2 clock<12> R2002	State Reject Difference Difference Accept Exclude	Revise State Accept Accept Accept	Trans ID TA1010 TA1011 TA1012 TA1100 TA1502 TA1412	Reference Provide the second s	Design Name: Object ID: Ce Designator: Part Name: Device Type: ackage name: Layer/Sheet: X Location: Y Location: otation (Deg): Pin Count: IP_NO_SWAP:	cell_phone_ra           U100           U100           SOIC16           MAX232           SOIC16           TOP           4225           3600           90           16           020-006-004           State           Difference           Reject	33       cell_phone_ra2         U100       U100         SOIC16       MAX232         SOIC16       TOP         4065       3064         0       16         020-006-004       Date / Time ▲         1/17/2007 1:11 AM       1/19/2007 2:04 PM
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## We are not alone!

## IDX file, a cooperative effort

- An open industry standard
- Based on XML schema
- Spans MCAD and ECAD definitions
- It does work, we are using it!

## Who are we working with?

- ProSTEP is the sponsor
- PTC is an active partner
- Mentor Graphics is an active partner
- Cadence is investigating
- Several EOMs and software vendors are participating as well















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